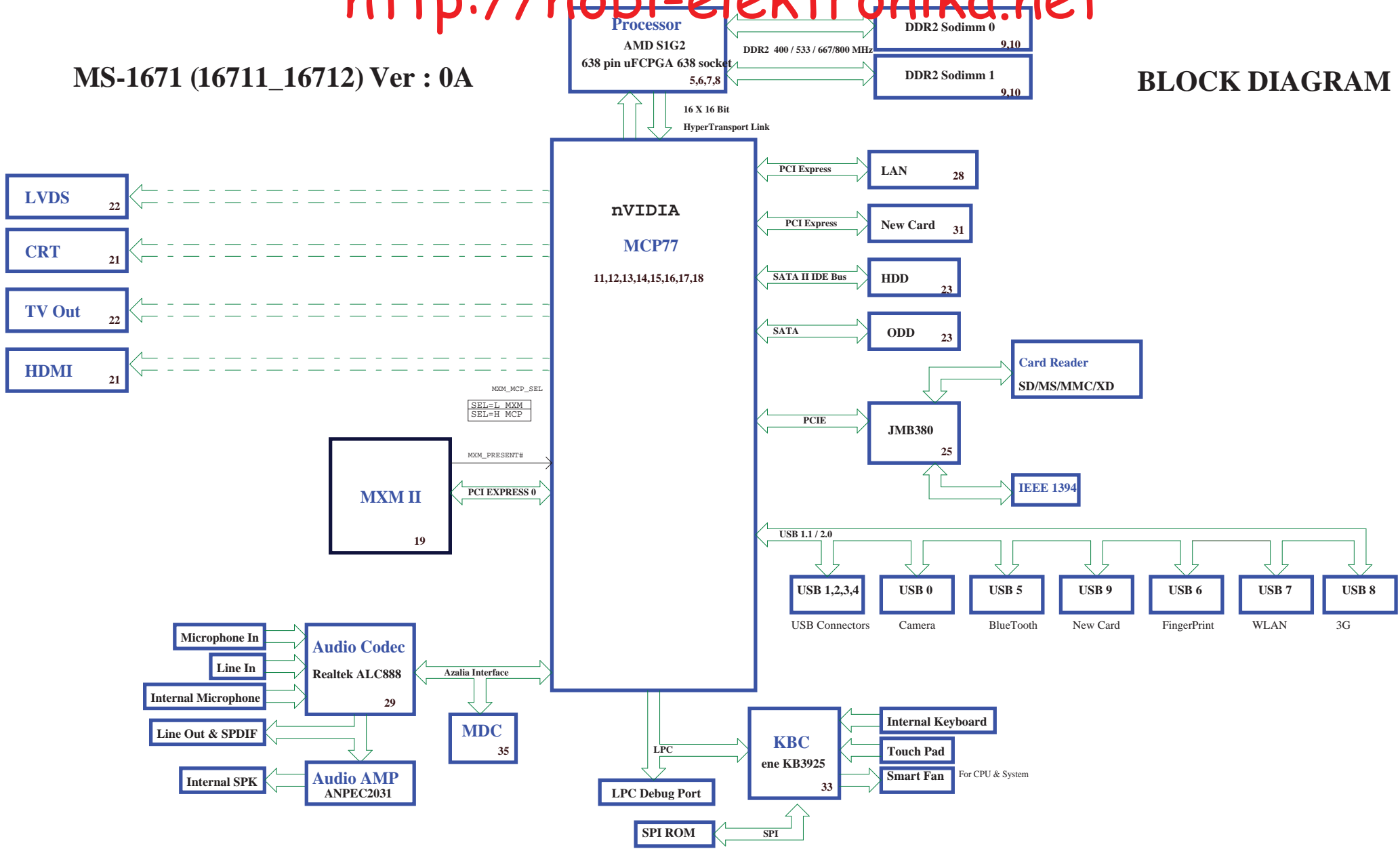
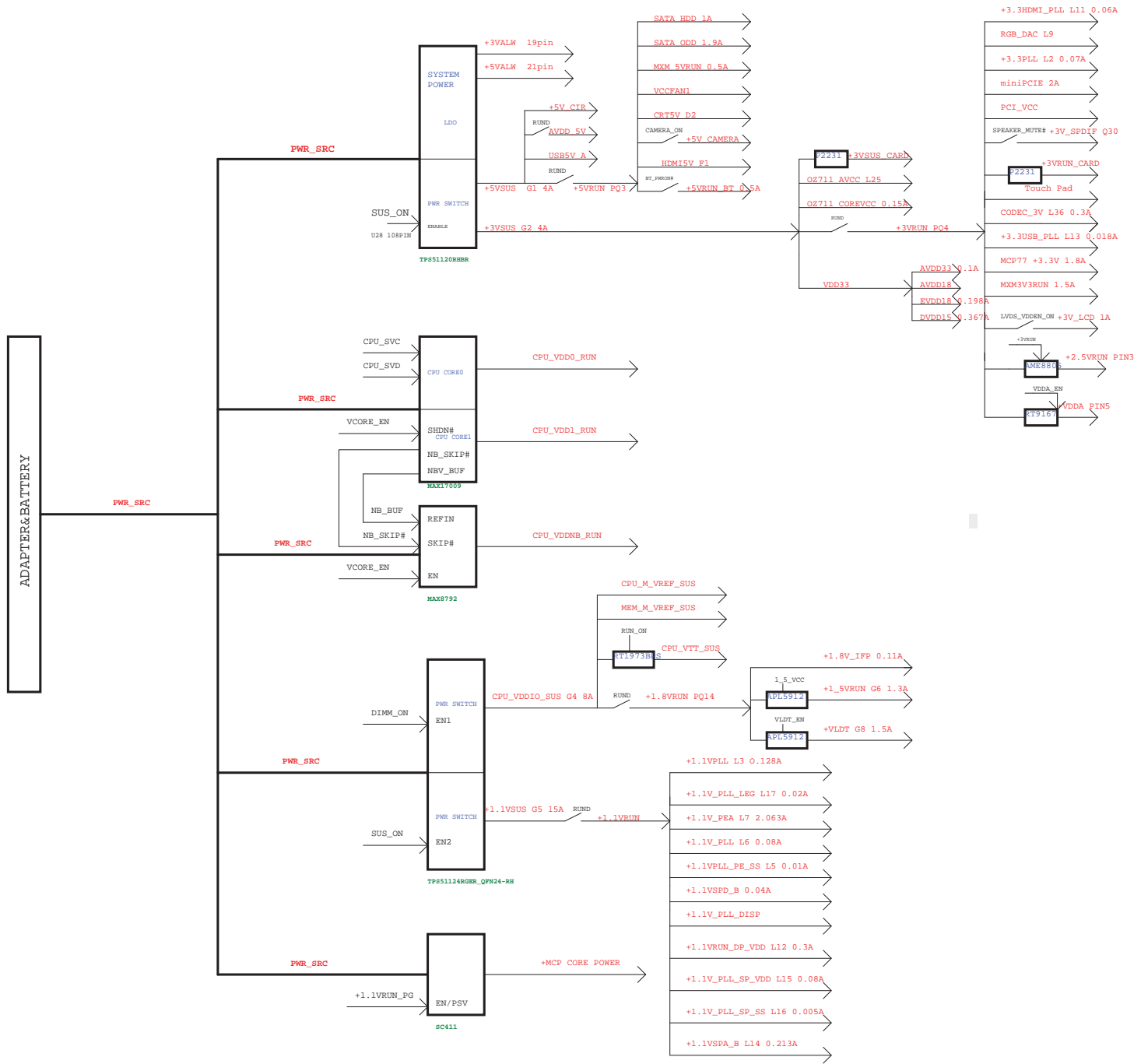
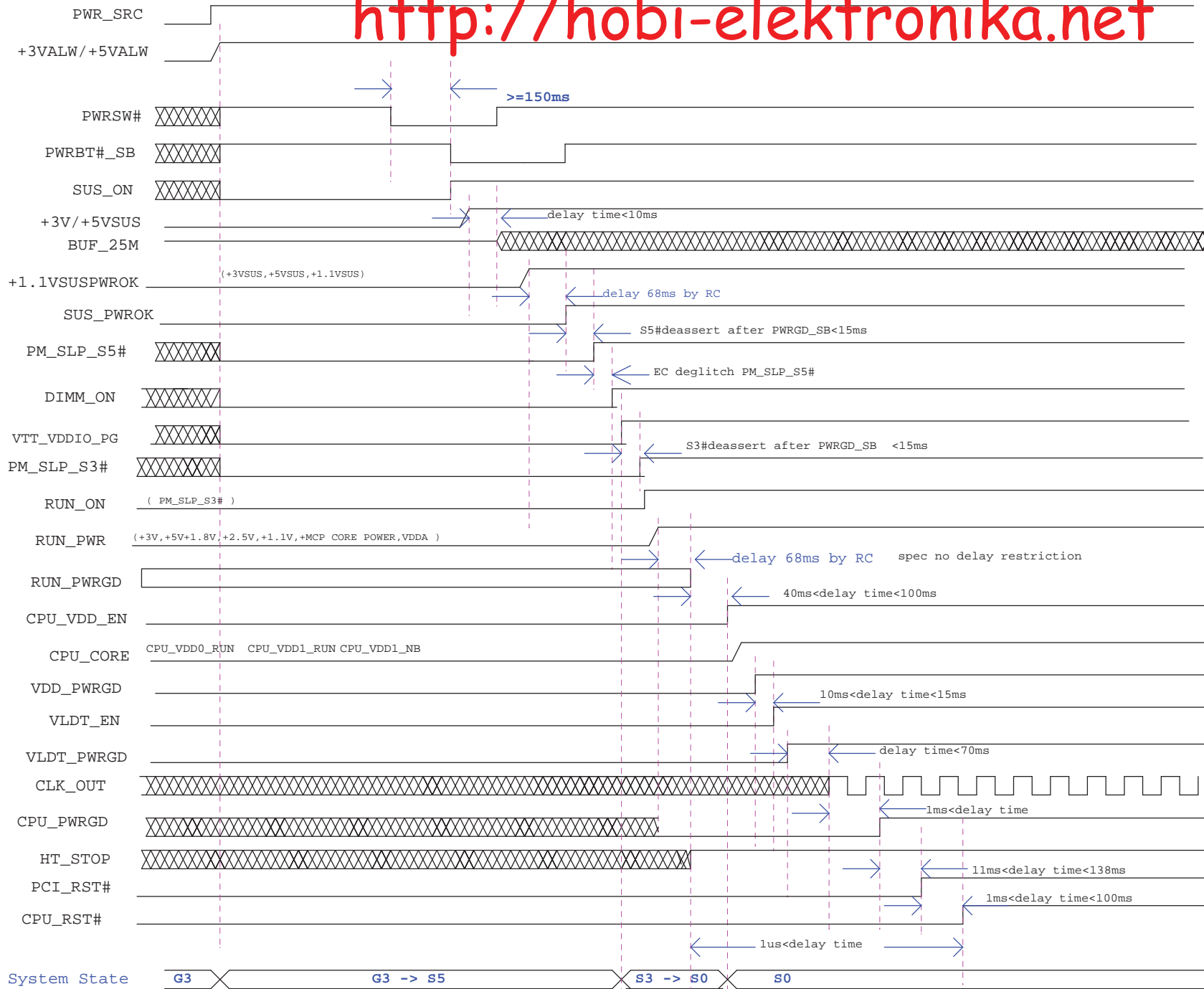


MS-1671 (16711\_16712) Ver : 0A


BLOCK DIAGRAM

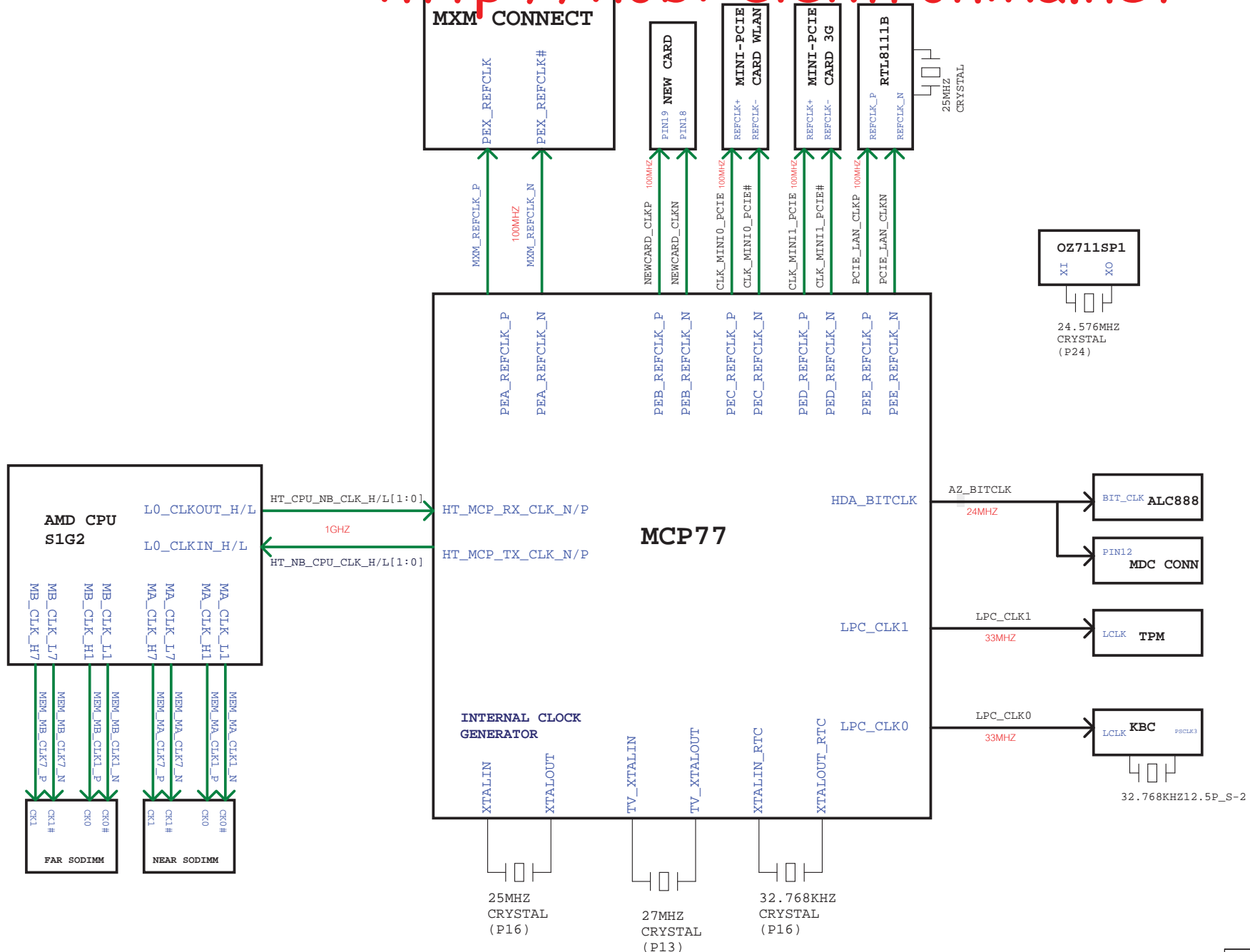


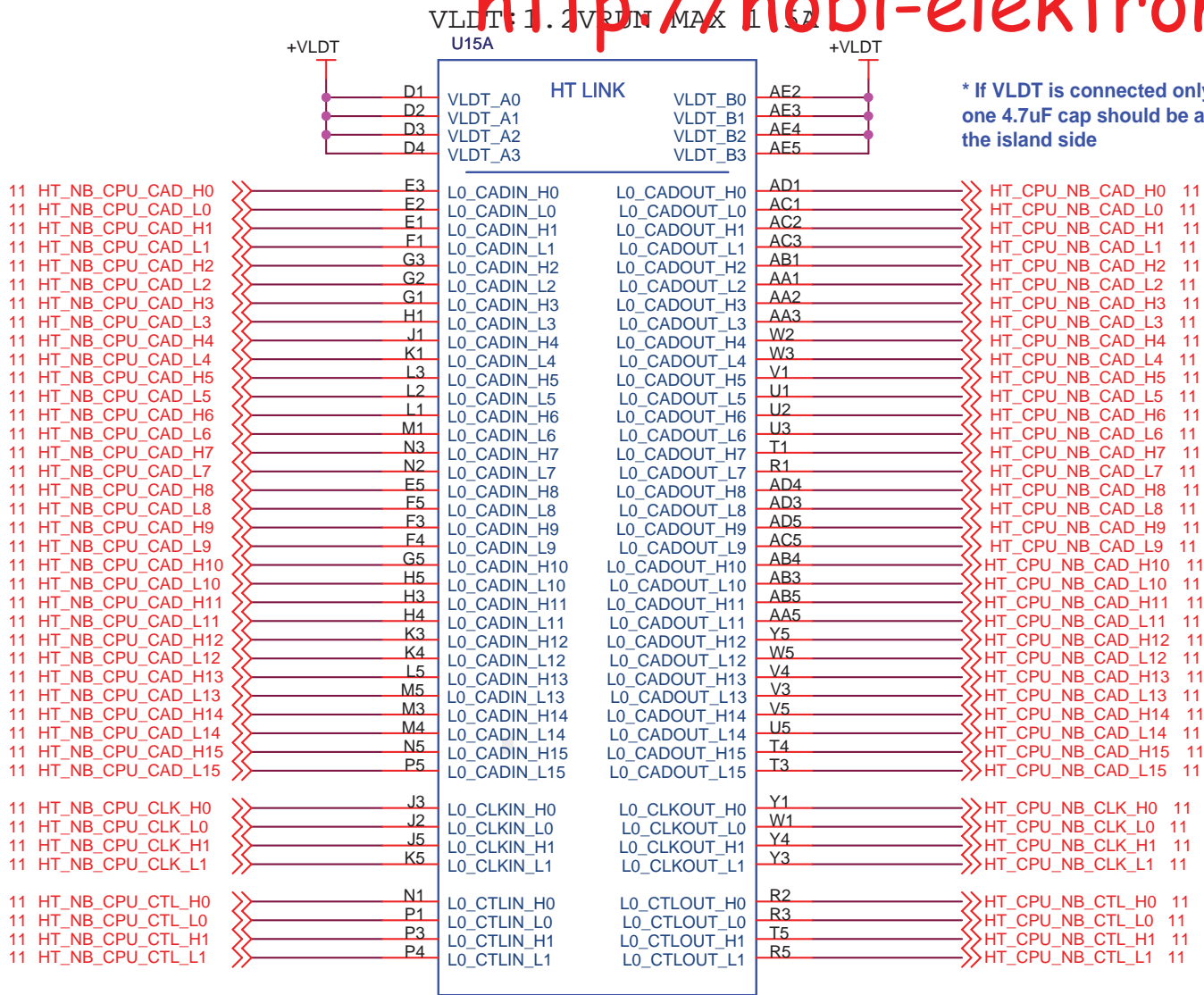




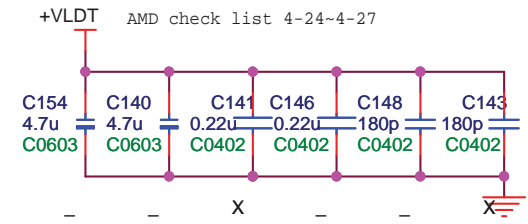
G3 -> S0 POWER UP SEQUENCE

 <b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>Title</b> POWER SEQUENCE	
<b>Size</b> Custom	<b>Document Number</b> MS-1671
<b>Date:</b> Friday, March 07, 2008	<b>Rev</b> 0A
Sheet 3 of 48	





\* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side



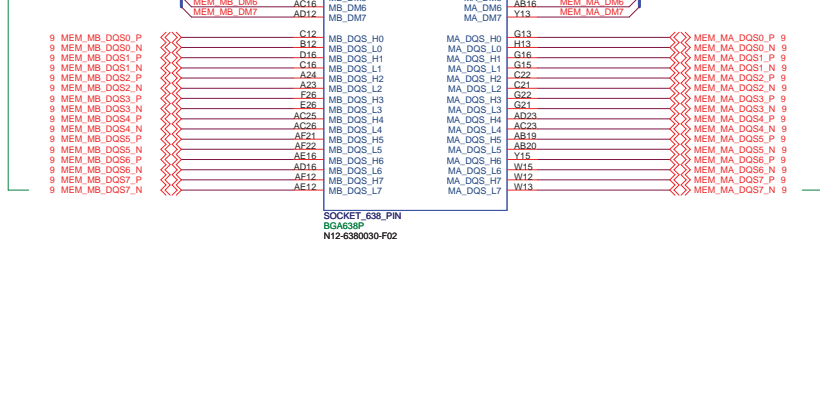
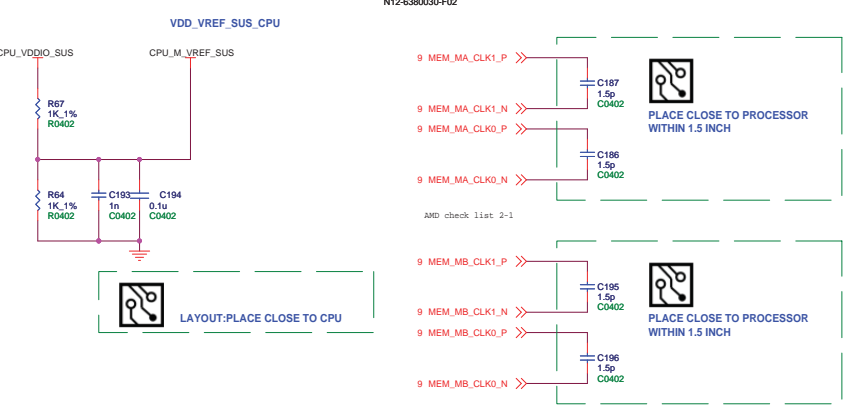
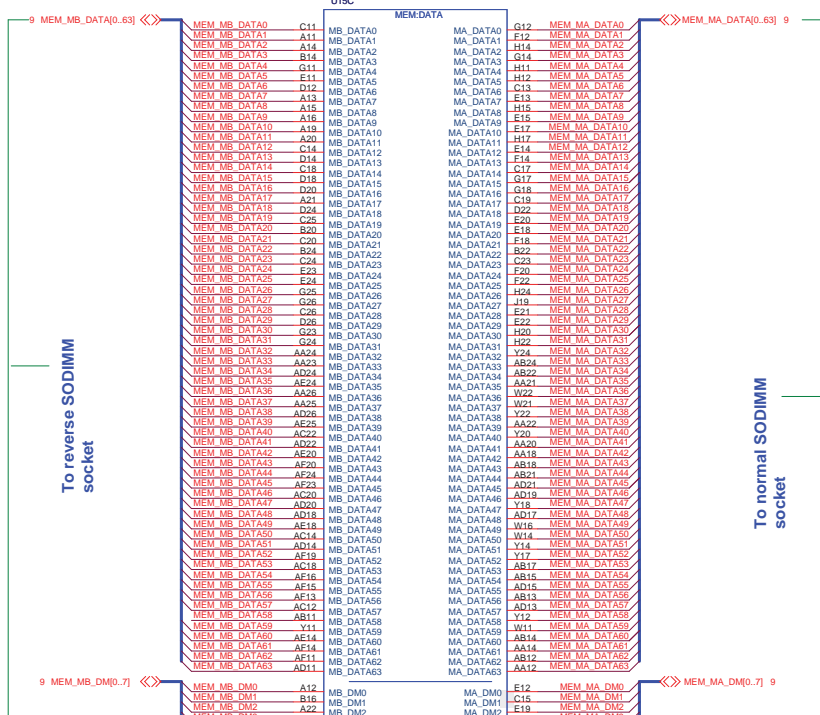
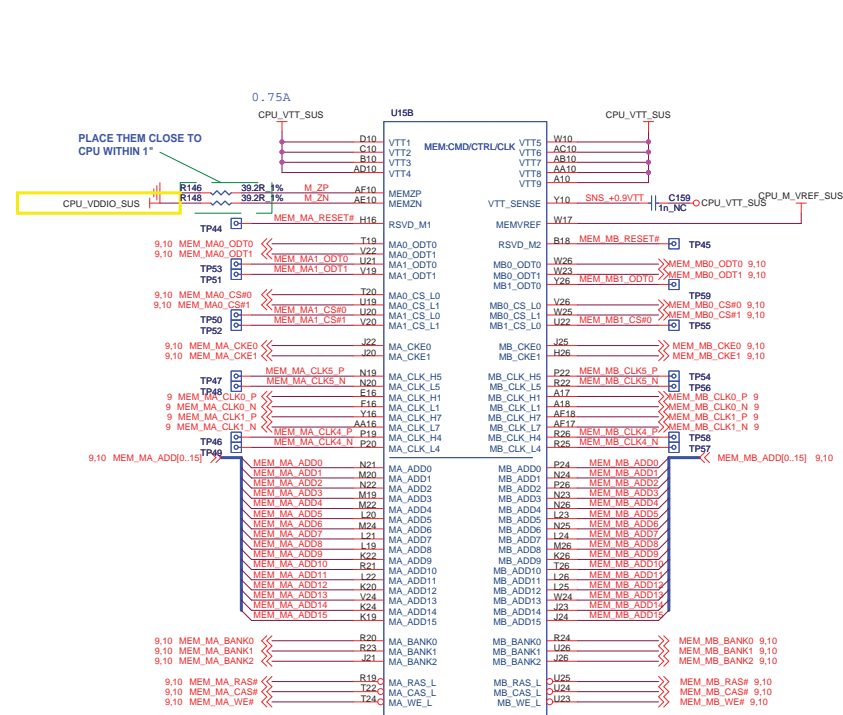
**LAYOUT: Place bypass cap on topside of board**  
 NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS  
 PLACE CLOSE TO VLDT0 POWER PINS



SOCKET\_638\_PIN  
 BGA638P  
 N12-6380030-F02

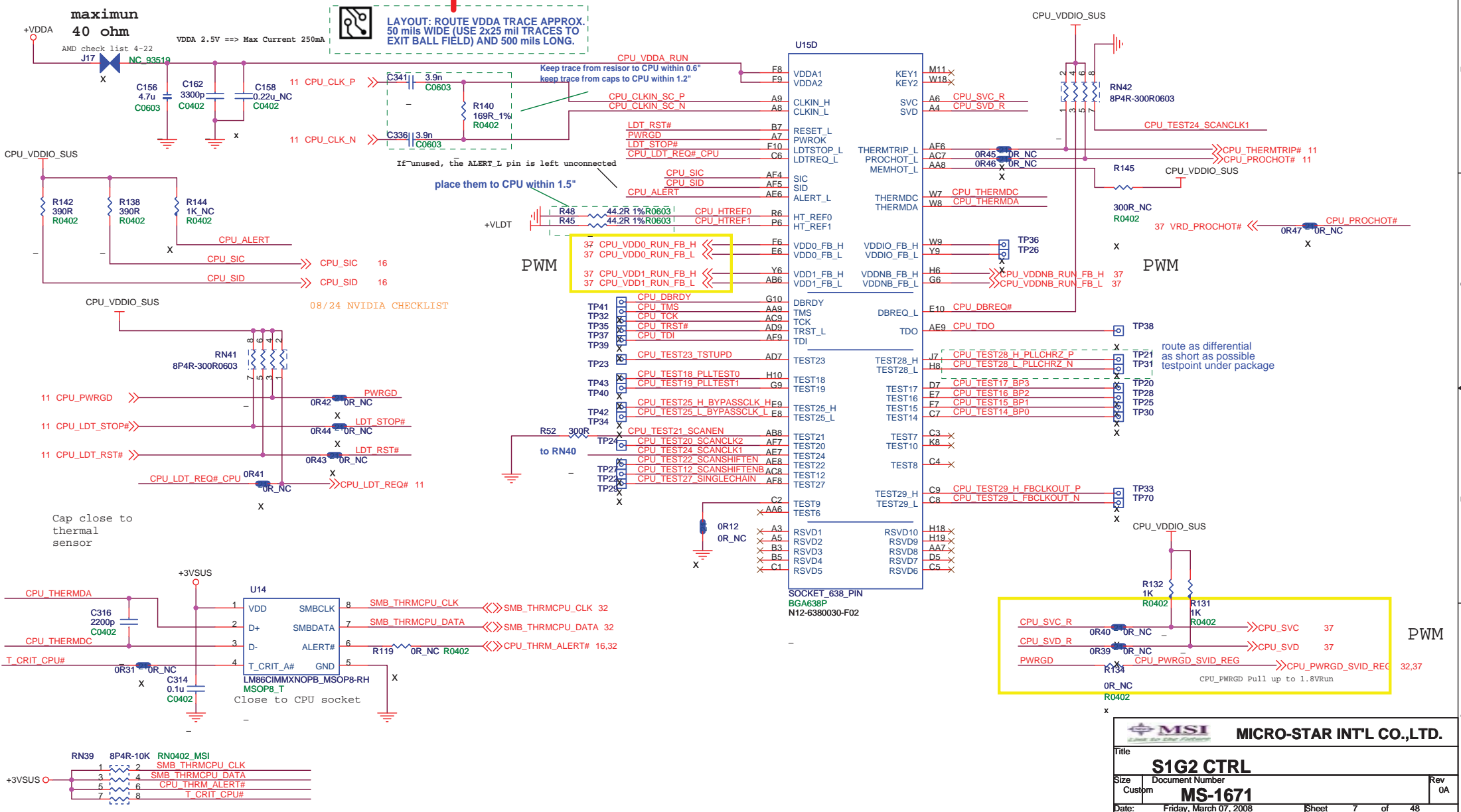
<b>MICRO-STAR INT'L CO.,LTD.</b>	
Title	
<b>S1G2 HT I/F</b>	
Size	Document Number
Custom	<b>MS-1671</b>
Date:	Friday, March 07, 2008
Sheet	5 of 48
Rev	0A

## Processor Memory Interface



## CPU\_VDDA 2.5V RUN

**LAYOUT: ROUTE VDDA TRACE APPROX 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.**



**MSI**  
MICRO-STAR INT'L CO.,LTD.

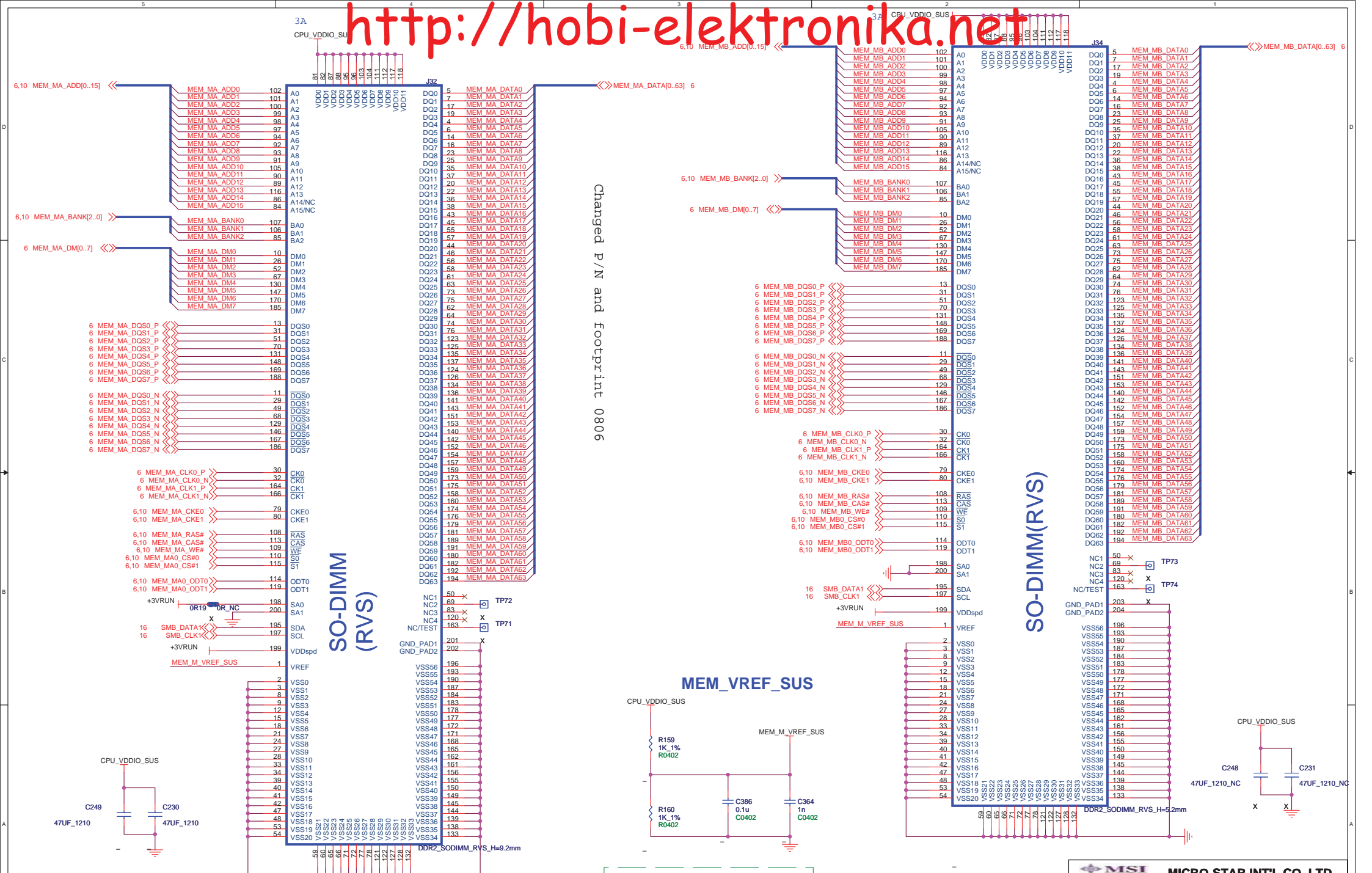
Title  
**S1G2 CTRL**

Size Document Number  
Custm **MS-1671**

Date: Friday, March 07, 2008 Sheet 7 of 48

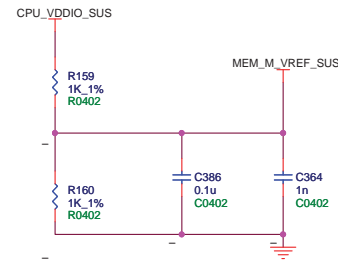






Changed P/N and Footprint 0806

### MEM\_VREF\_SUS



LAYOUT: PLACE CLOSE TO DIMMS

### SO-DIMM(RVS)

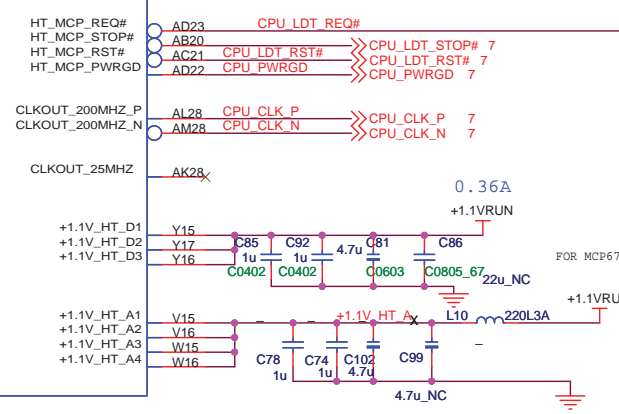
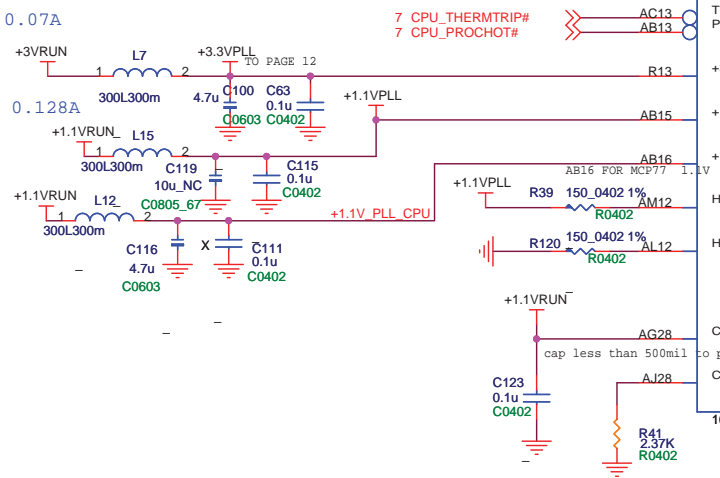
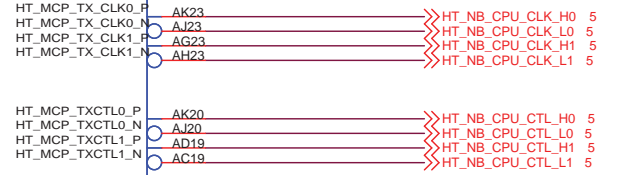
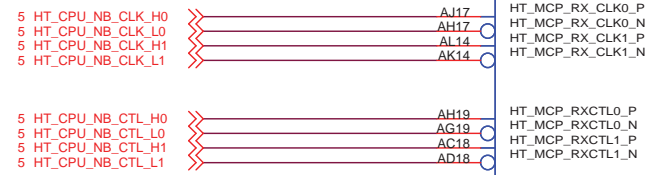
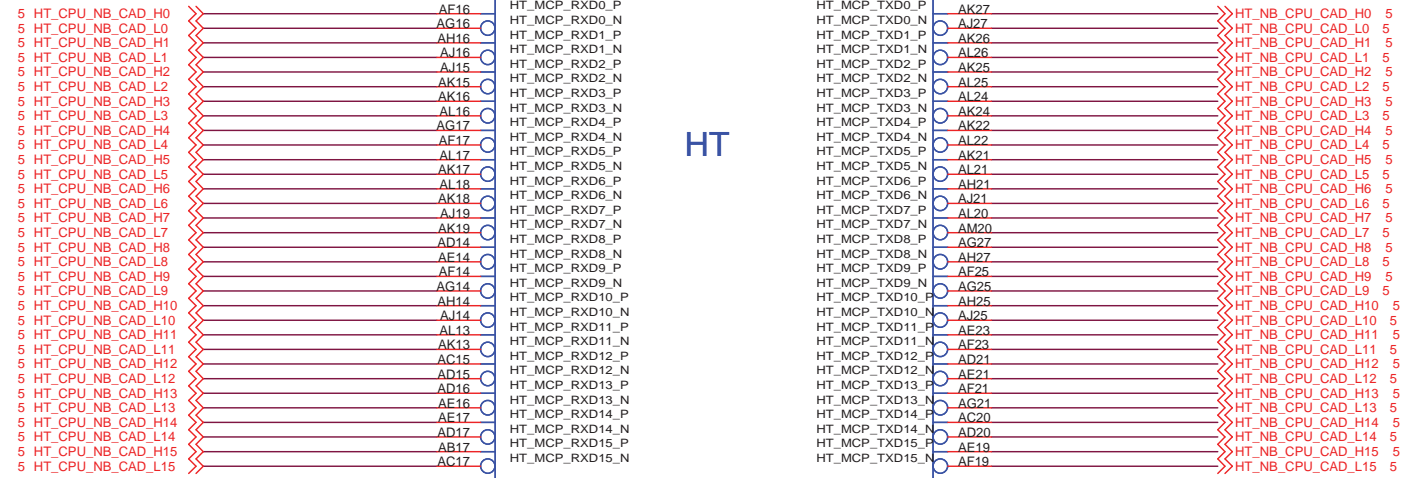
		MICRO-STAR INT'L CO.,LTD.	
Title: <b>DDR2 SODIMMS:A/B CHANNEL</b>			
Size: Custom		Document Number: <b>MS-1671</b>	
Date: Friday, March 07, 2008		Sheet 9 of 48	




U12  
MCP77  
PBGA836

SEC 1 OF 8

HT

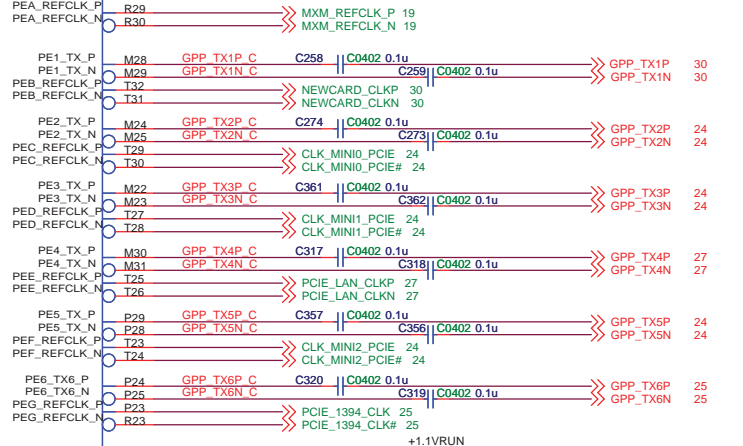
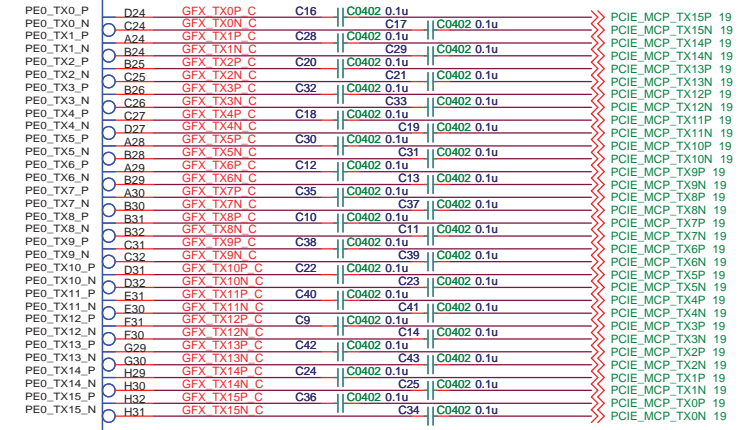
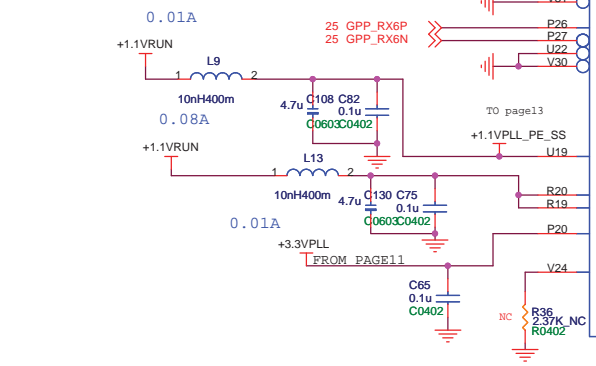
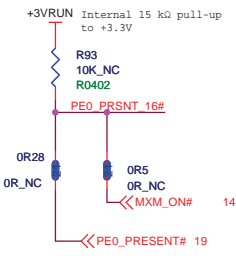
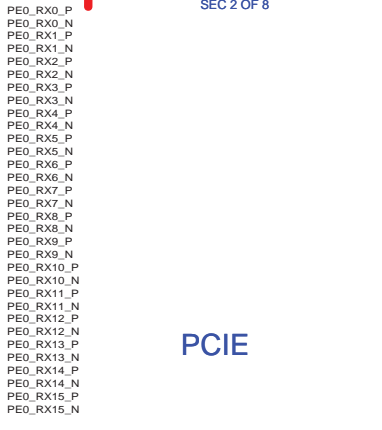
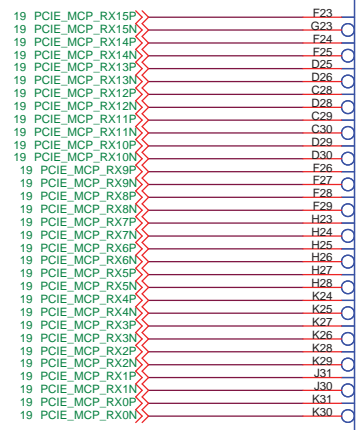


Delete level shift MOS  
1227 ref  
3346-001\_v04

		<b>MICRO-STAR INT'L CO.,LTD.</b>	
Title			
<b>MCP77-HT LINK0 I/F</b>			
Size	Document Number		Rev
B	<b>MS-1671</b>		0A
Date:	Friday, March 07, 2008	Sheet	11 of 48

## SEC 2 OF 8

## PCIE



U12C  
MCP77  
PBG8A86

SEC 3 OF 8  
**LAN**

RGMIIL\_RXD0MII\_RXD0  
RGMIIL\_RXD1MII\_RXD1  
RGMIIL\_RXD2MII\_RXD2  
RGMIIL\_RXD3MII\_RXD3  
RGMIIL\_RXCMII\_RXCLK  
RGMIIL\_RXCTLII\_RXDVI  
MII\_RXERGPIO\_36  
MII\_COL\_NSMIB\_DATA  
MII\_CRS/MSMB\_CLK  
RGMIIMII\_INTR/GPIO35  
MII\_COMP\_3P3V  
MII\_COMP\_GND  
MII\_RESETI  
MII\_VREFI

**DACS**  
RGB\_DAC\_REBI  
RGB\_DAC\_RSETI  
RGB\_DAC\_VREFI  
RGB\_DAC\_BLUEI  
RGB\_DAC\_HSYNCI  
RGB\_DAC\_VSYNCI  
DDC\_CLKI  
DDC\_DATAI  
TV\_XTALIN  
TV\_XTALOUT  
+3.3V\_TV\_DACI  
TV\_DAC\_REDI  
TV\_DAC\_GREENI  
TV\_DAC\_BLUEI  
IFPA\_TXC\_P  
IFPA\_TXC\_N

GPIO\_6/FERR/SYS\_SERR/IGPU\_GPIO\_6\*  
GPIO\_7/FERR/SYS\_PERR/IGPU\_GPIO\_7\*  
LCD\_BKL\_CTLI  
LCD\_BKL\_ONI  
LCD\_PANEL\_PWRI  
HDMI\_CP\_MCP  
HDMI\_CN\_MCP  
HDMI\_D0P\_MCP  
HDMI\_D0N\_MCP  
HDMI\_D1P\_MCP  
HDMI\_D1N\_MCP  
HDMI\_D2P\_MCP  
HDMI\_D2N\_MCP

**FLAT PANEL**  
HDMI\_TXC\_PIMLO\_LANE3\_P  
HDMI\_TXC\_NIMLO\_LANE3\_N  
HDMI\_TXD0\_PIMLO\_LANE2\_P  
HDMI\_TXD0\_NIMLO\_LANE2\_N  
HDMI\_TXD1\_PIMLO\_LANE1\_P  
HDMI\_TXD1\_NIMLO\_LANE1\_N  
HDMI\_TXD2\_PIMLO\_LANE0\_P  
HDMI\_TXD2\_NIMLO\_LANE0\_N  
AUX\_CH0\_P  
AUX\_CH0\_N  
HPLUG\_DET3  
HPLUG\_DET2  
+1.8V\_IFPAB  
+1.8V\_IFPB  
+3.3V\_IFPAB\_HVDD  
+3.3V\_HDMI\_PLL\_HVDD  
+1.1V\_PLL\_DP  
+1.1V\_DP\_VDD  
HDMI\_RSETI  
HDMI\_VPROBEI

IFPA\_TXC\_P  
IFPA\_TXC\_N  
IFPB\_TXD0\_P  
IFPB\_TXD0\_N  
IFPB\_TXD1\_P  
IFPB\_TXD1\_N  
IFPB\_TXD2\_P  
IFPB\_TXD2\_N  
IFPB\_TXD3\_P  
IFPB\_TXD3\_N  
IFPB\_TXD4\_P  
IFPB\_TXD4\_N  
IFPB\_TXD6\_P  
IFPB\_TXD6\_N  
IFPB\_TXD7\_P  
IFPB\_TXD7\_N  
DDC\_CLKI  
DDC\_DATAI  
DDC\_CLKI  
DDC\_DATAI  
IFPAB\_RSETI  
IFPAB\_VPROBEI

16XXX  
MCP77 NC  
C322 0.1uF NC  
R125 1K\_1% NC  
R0402

GROUNDING RMGT POWER. wait nvidia response

RGMIIL\_TXD0MII\_TXD0  
RGMIIL\_TXD1MII\_TXD1  
RGMIIL\_TXD2MII\_TXD2  
RGMIIL\_TXD3MII\_TXD3  
RGMIIL\_TXCLKMII\_TXCLK  
RGMIIL\_TXCTLMII\_TXN  
RGMIIMII\_MDCI  
RGMIIMII\_MDIOI  
BUF\_25MHZ  
MII\_VREFI  
RGMIIL\_TXD0MII\_TXD0  
RGMIIL\_TXD1MII\_TXD1  
RGMIIL\_TXD2MII\_TXD2  
RGMIIL\_TXD3MII\_TXD3  
RGMIIL\_TXCLKMII\_TXCLK  
RGMIIL\_TXCTLMII\_TXN  
RGMIIMII\_MDCI  
RGMIIMII\_MDIOI  
MII\_VREFI

VGA\_R\_MCP  
VGA\_G\_MCP  
VGA\_B\_MCP  
HSYNC\_MCP  
VSYNC\_MCP  
CRT\_CLK\_MCP  
CRT\_DATA\_MCP  
+3VRUN  
L2 220L3A  
C55 0.1uF\_0402  
C64 0.1uF\_0402  
C61 4.7u\_0805\_X5R  
RG1 150\_1%\_0402  
RG3 150\_1%\_0402  
RG2 150\_1%\_0402

LVDS\_TXCLKP\_MCP  
LVDS\_TXCLKN\_MCP  
LVDS\_TXL0P\_MCP  
LVDS\_TXL0N\_MCP  
LVDS\_TXL1P\_MCP  
LVDS\_TXL1N\_MCP  
LVDS\_TXL2P\_MCP  
LVDS\_TXL2N\_MCP  
LVDS\_TXU0P\_MCP  
LVDS\_TXU0N\_MCP  
LVDS\_TXU1P\_MCP  
LVDS\_TXU1N\_MCP  
LVDS\_TXU2P\_MCP  
LVDS\_TXU2N\_MCP

LVDS\_TXCLKP\_MCP  
LVDS\_TXCLKN\_MCP  
LVDS\_TXL0P\_MCP  
LVDS\_TXL0N\_MCP  
LVDS\_TXL1P\_MCP  
LVDS\_TXL1N\_MCP  
LVDS\_TXL2P\_MCP  
LVDS\_TXL2N\_MCP  
LVDS\_TXU0P\_MCP  
LVDS\_TXU0N\_MCP  
LVDS\_TXU1P\_MCP  
LVDS\_TXU1N\_MCP  
LVDS\_TXU2P\_MCP  
LVDS\_TXU2N\_MCP

LVDS\_TXCLKP\_MCP  
LVDS\_TXCLKN\_MCP  
LVDS\_TXL0P\_MCP  
LVDS\_TXL0N\_MCP  
LVDS\_TXL1P\_MCP  
LVDS\_TXL1N\_MCP  
LVDS\_TXL2P\_MCP  
LVDS\_TXL2N\_MCP  
LVDS\_TXU0P\_MCP  
LVDS\_TXU0N\_MCP  
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LVDS\_TXU2P\_MCP  
LVDS\_TXU2N\_MCP

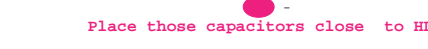
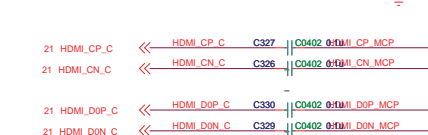
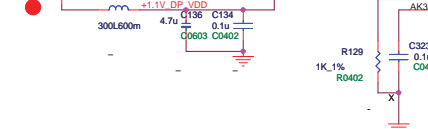
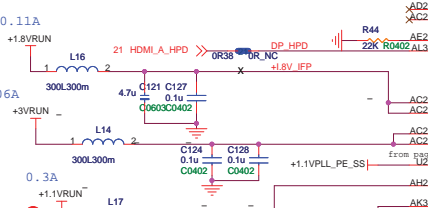
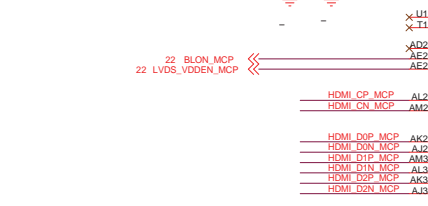
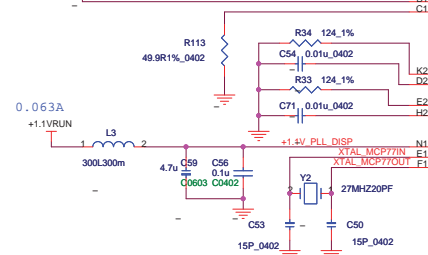
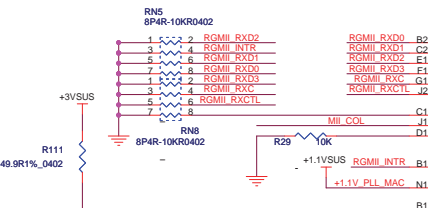
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LVDS\_TXCLKN\_MCP  
LVDS\_TXL0P\_MCP  
LVDS\_TXL0N\_MCP  
LVDS\_TXL1P\_MCP  
LVDS\_TXL1N\_MCP  
LVDS\_TXL2P\_MCP  
LVDS\_TXL2N\_MCP  
LVDS\_TXU0P\_MCP  
LVDS\_TXU0N\_MCP  
LVDS\_TXU1P\_MCP  
LVDS\_TXU1N\_MCP  
LVDS\_TXU2P\_MCP  
LVDS\_TXU2N\_MCP

LVDS\_TXCLKP\_MCP  
LVDS\_TXCLKN\_MCP  
LVDS\_TXL0P\_MCP  
LVDS\_TXL0N\_MCP  
LVDS\_TXL1P\_MCP  
LVDS\_TXL1N\_MCP  
LVDS\_TXL2P\_MCP  
LVDS\_TXL2N\_MCP  
LVDS\_TXU0P\_MCP  
LVDS\_TXU0N\_MCP  
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LVDS\_TXU2N\_MCP

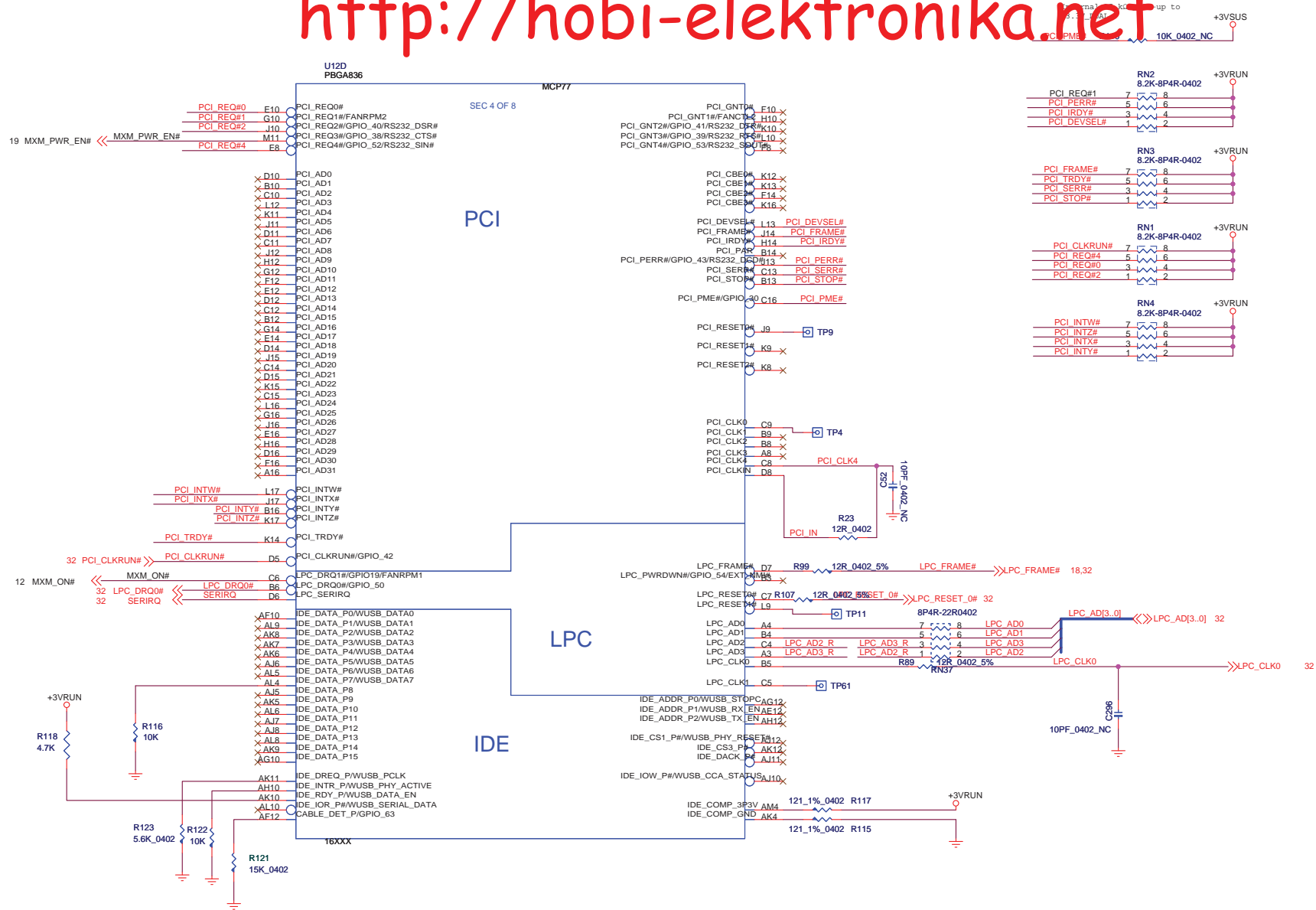
LVDS\_TXCLKP\_MCP  
LVDS\_TXCLKN\_MCP  
LVDS\_TXL0P\_MCP  
LVDS\_TXL0N\_MCP  
LVDS\_TXL1P\_MCP  
LVDS\_TXL1N\_MCP  
LVDS\_TXL2P\_MCP  
LVDS\_TXL2N\_MCP  
LVDS\_TXU0P\_MCP  
LVDS\_TXU0N\_MCP  
LVDS\_TXU1P\_MCP  
LVDS\_TXU1N\_MCP  
LVDS\_TXU2P\_MCP  
LVDS\_TXU2N\_MCP

LVDS\_TXCLKP\_MCP  
LVDS\_TXCLKN\_MCP  
LVDS\_TXL0P\_MCP  
LVDS\_TXL0N\_MCP  
LVDS\_TXL1P\_MCP  
LVDS\_TXL1N\_MCP  
LVDS\_TXL2P\_MCP  
LVDS\_TXL2N\_MCP  
LVDS\_TXU0P\_MCP  
LVDS\_TXU0N\_MCP  
LVDS\_TXU1P\_MCP  
LVDS\_TXU1N\_MCP  
LVDS\_TXU2P\_MCP  
LVDS\_TXU2N\_MCP

LVDS\_TXCLKP\_MCP  
LVDS\_TXCLKN\_MCP  
LVDS\_TXL0P\_MCP  
LVDS\_TXL0N\_MCP  
LVDS\_TXL1P\_MCP  
LVDS\_TXL1N\_MCP  
LVDS\_TXL2P\_MCP  
LVDS\_TXL2N\_MCP  
LVDS\_TXU0P\_MCP  
LVDS\_TXU0N\_MCP  
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LVDS\_TXU2N\_MCP

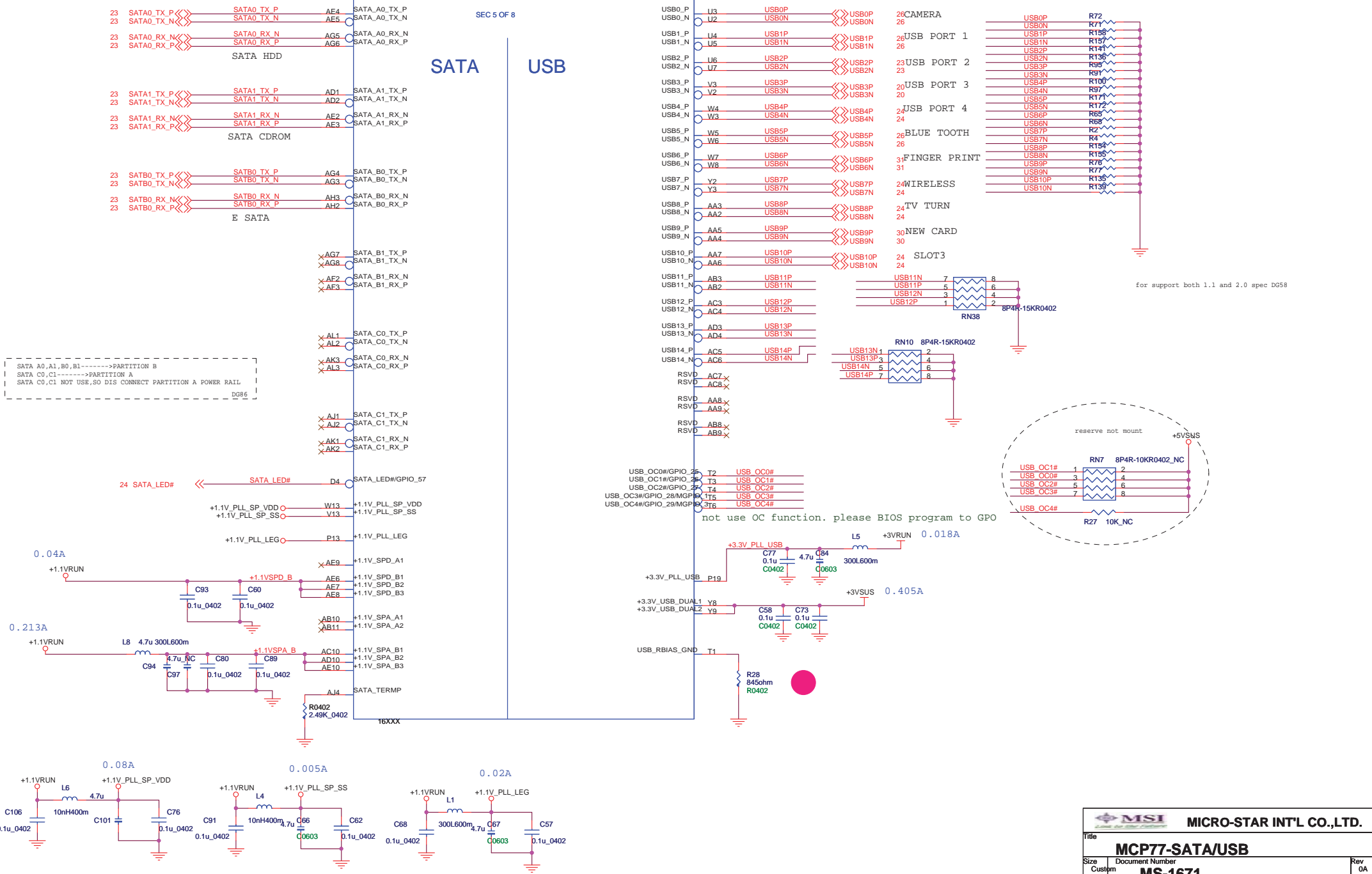


Place those capacitors close to HDMI connector

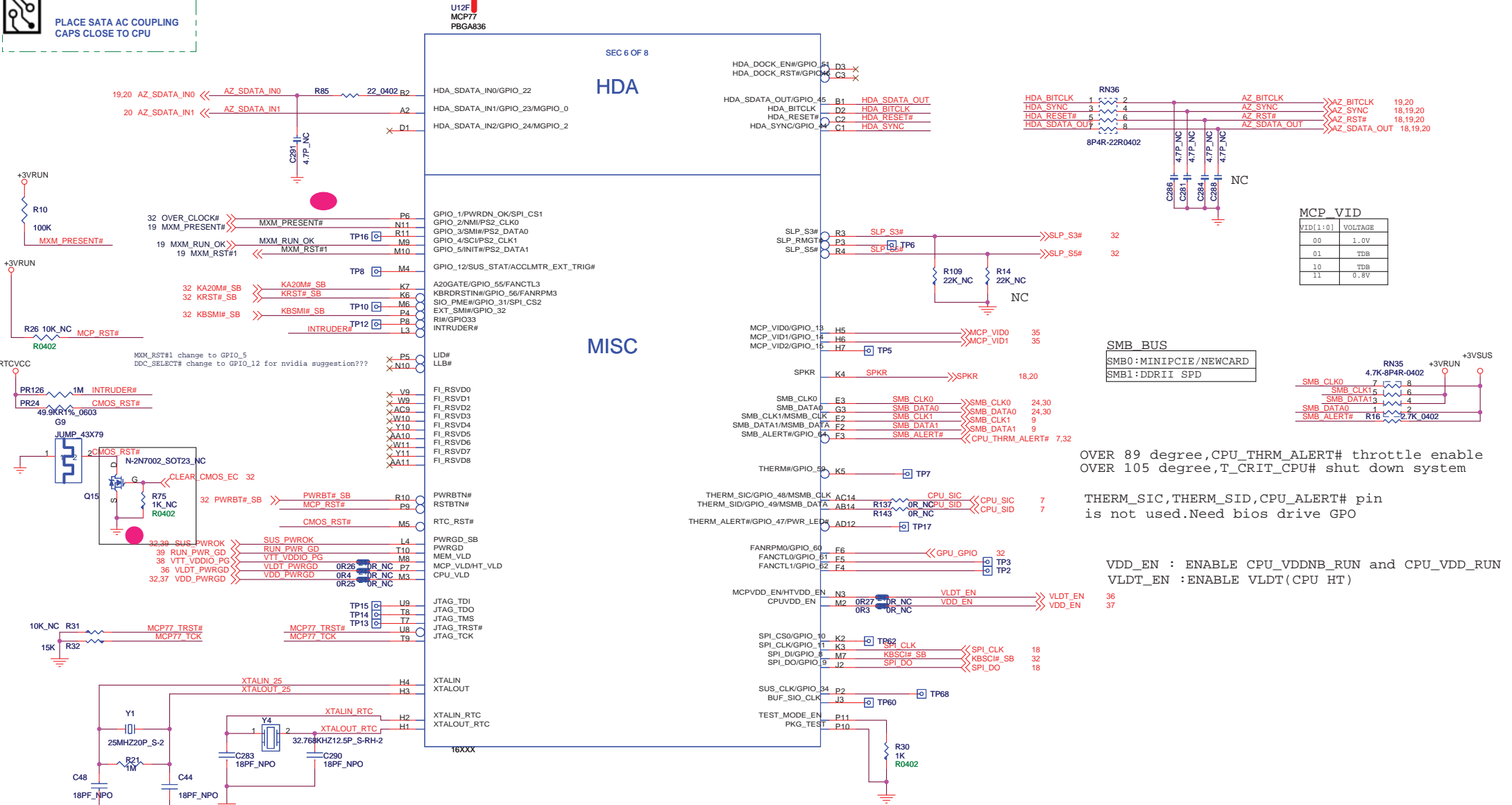




U12E  
MCP77  
PBG836



PLACE SATA AC COUPLING CAPS CLOSE TO CPU



MCP VID

VID[1:0]	VOLTAGE
00	1.0V
01	TDB
10	TDB
11	0.8V

SMB BUS  
SMB0:MINIPICIE/NEWCARD  
SMB1:DDRII SPD

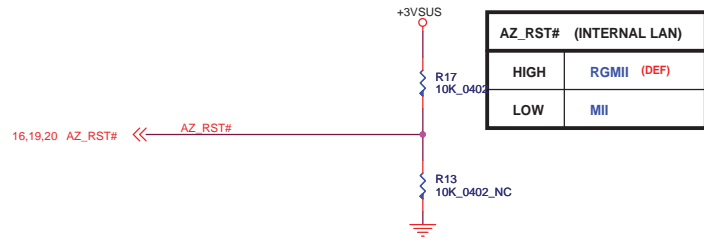
OVER 89 degree,CPU\_THRM\_ALERT# throttle enable  
OVER 105 degree,T\_CRIT\_CPU# shut down system

THERM\_SIC,THERM\_SID,CPU\_ALERT# pin is not used.Need bios drive GPO

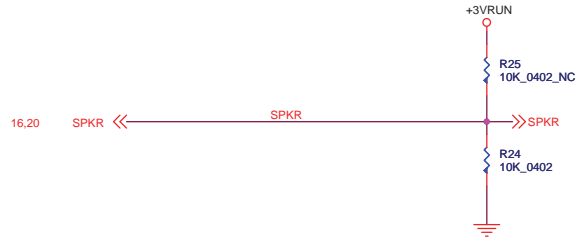
VDD\_EN : ENABLE CPU\_VDDNB\_RUN and CPU\_VDD\_RUN  
VLDT\_EN :ENABLE VLDT(CPU HT)



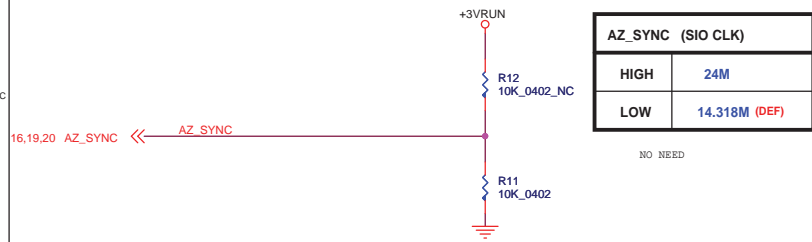




AZ_RST# (INTERNAL LAN)	
HIGH	RGMI (DEF)
LOW	MII

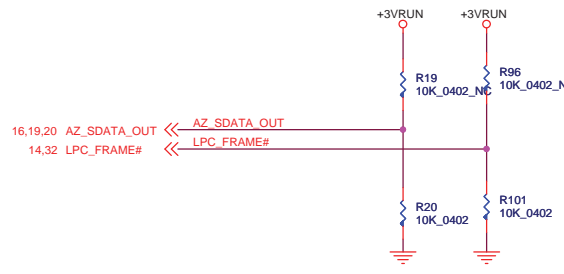


ROM TABLE (SPEAKER)	
HIGH	SAFE
LOW	USER (DEF)

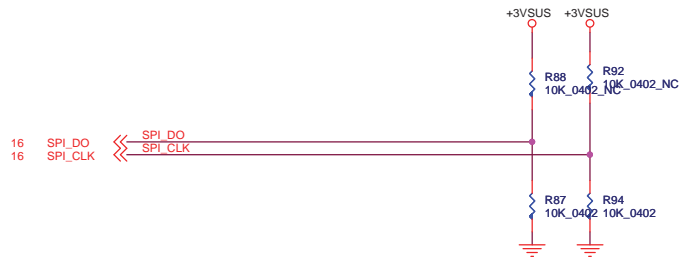


AZ_SYNC (SIO CLK)	
HIGH	24M
LOW	14.318M (DEF)

NO NEED

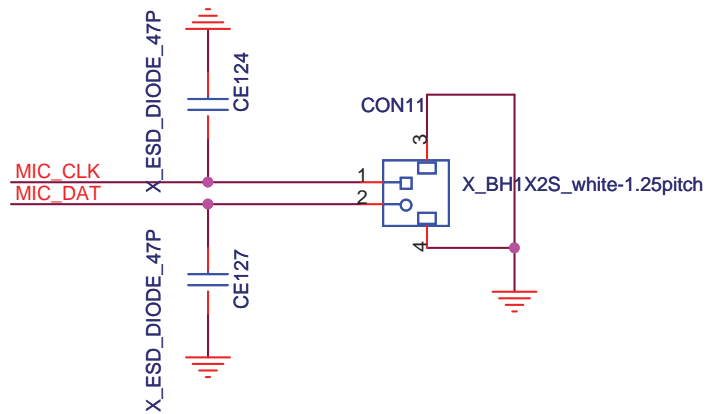
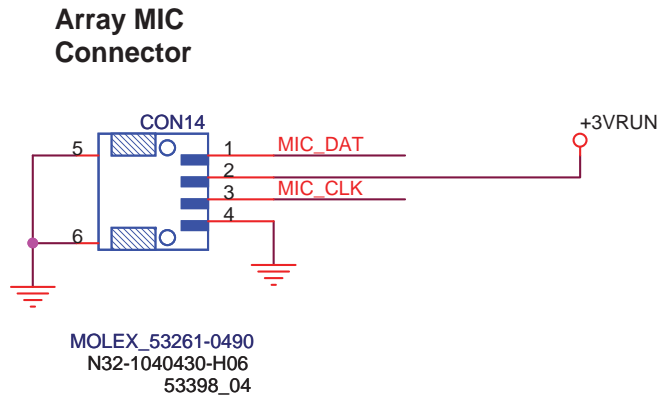
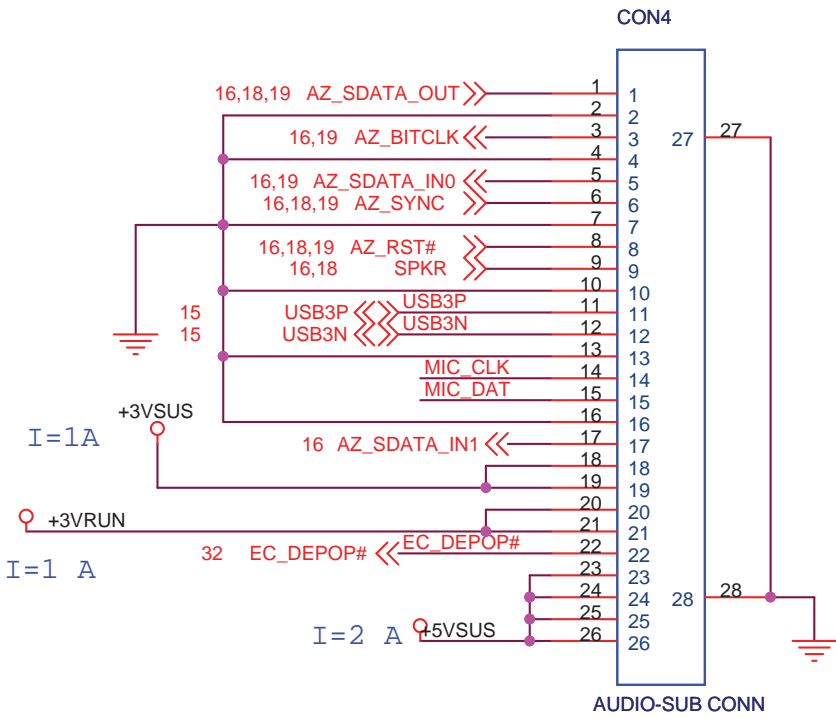



AZ_SDATA_OUT(H)/LPC_FRAME#(L)	
00	LPC BIOS (DEF)
01	PCI BIOS
10	SPI BIOS
11	RESERVE

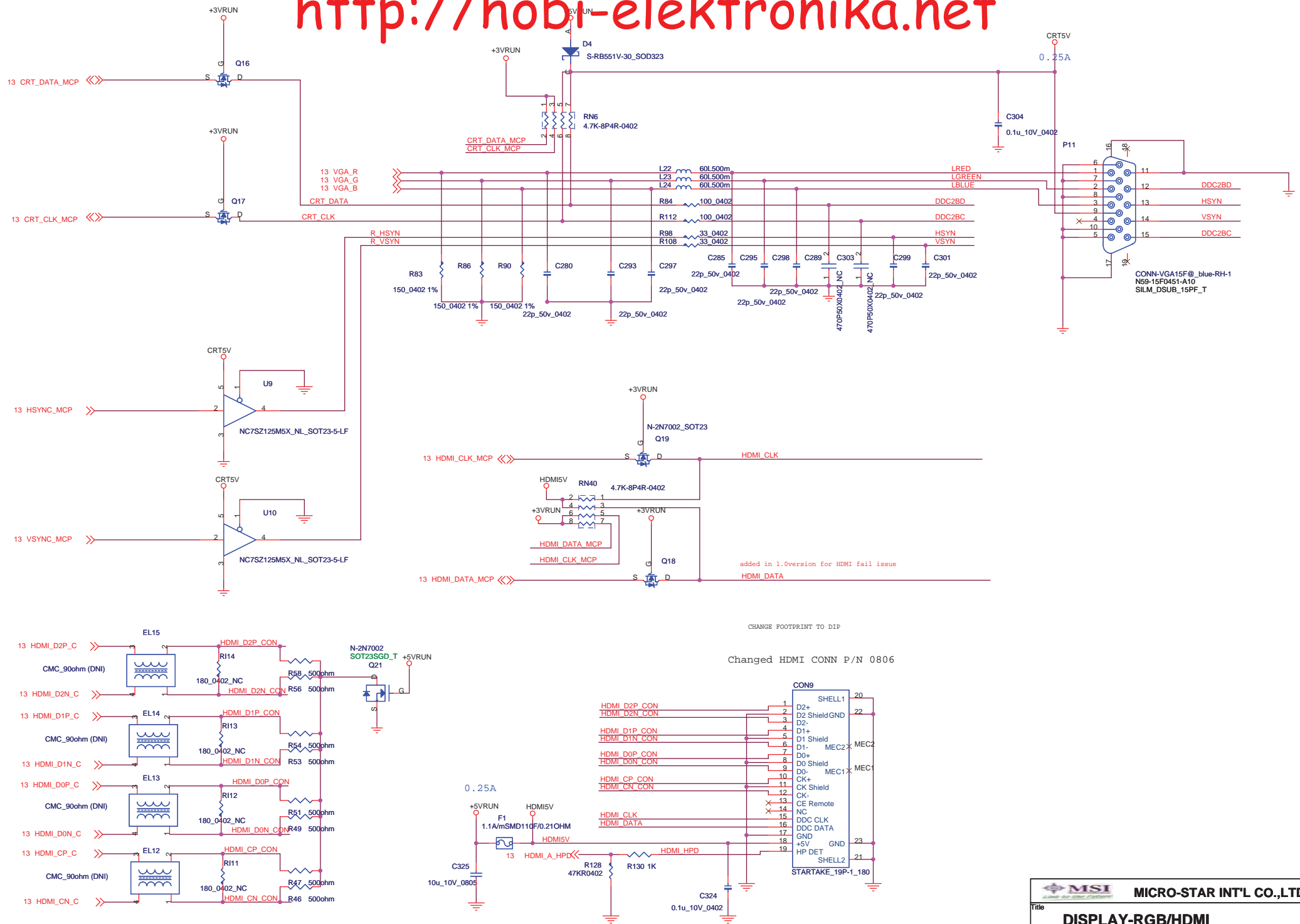


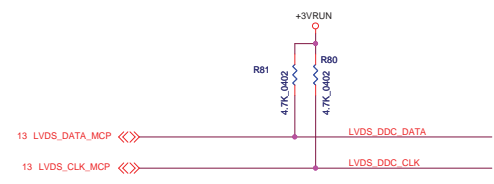
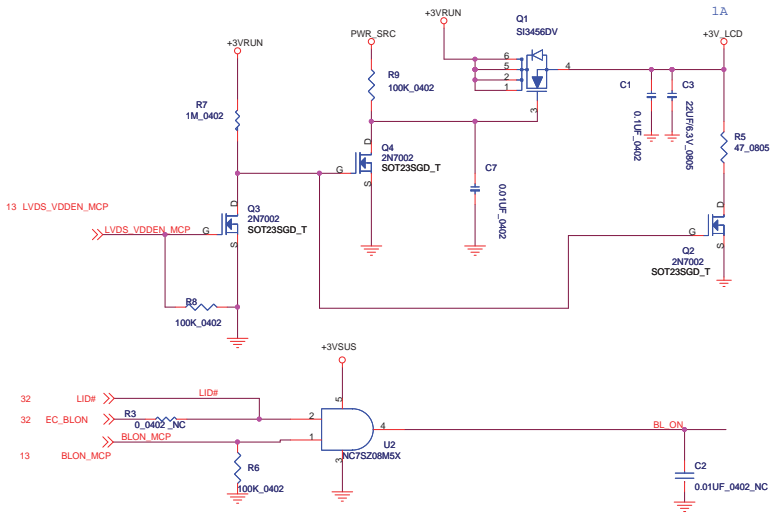
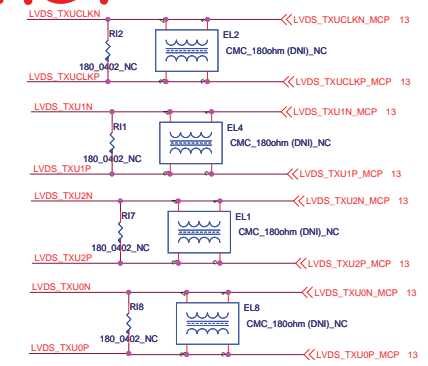
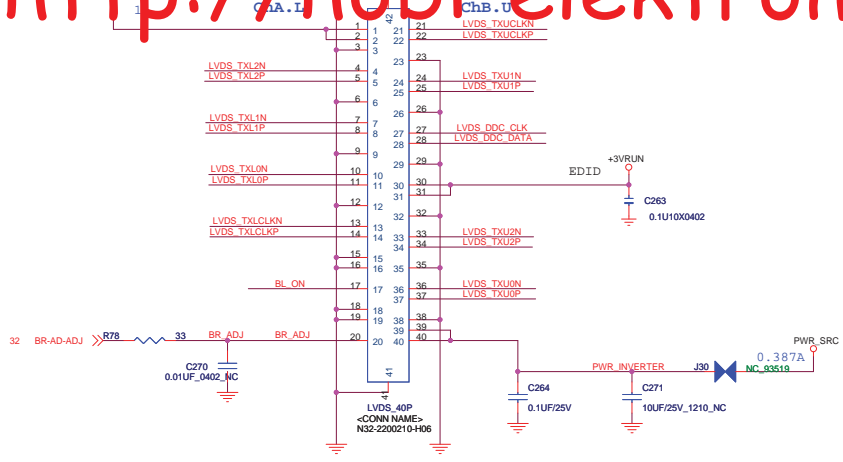
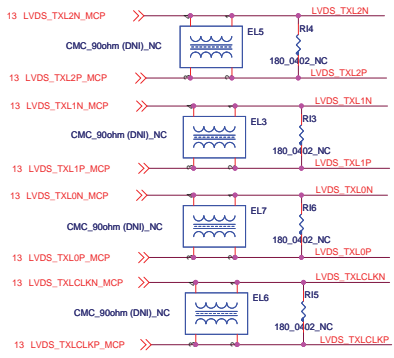
SPI_DO(H)/SPI_CLK(L)	
00	31MHZ (DEF)
01	RESERVED
10	25MHZ
11	1MHZ

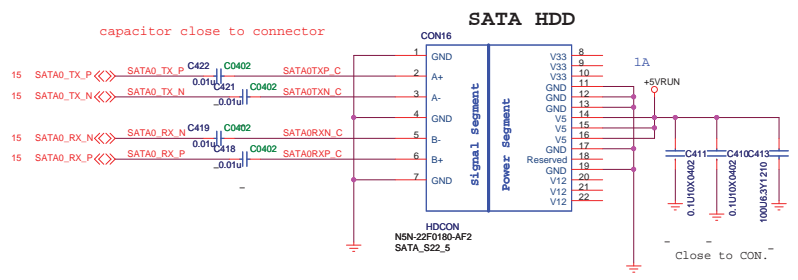
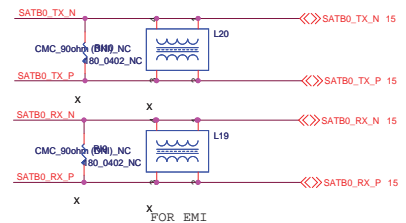
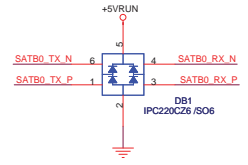
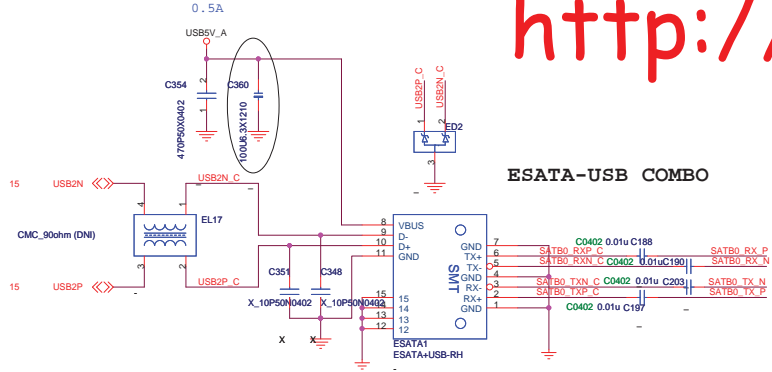




 <b>MICRO-STAR INT'L CO.,LTD.</b>	
Title	
<b>AUDIO&amp;USB CONNECTOR</b>	
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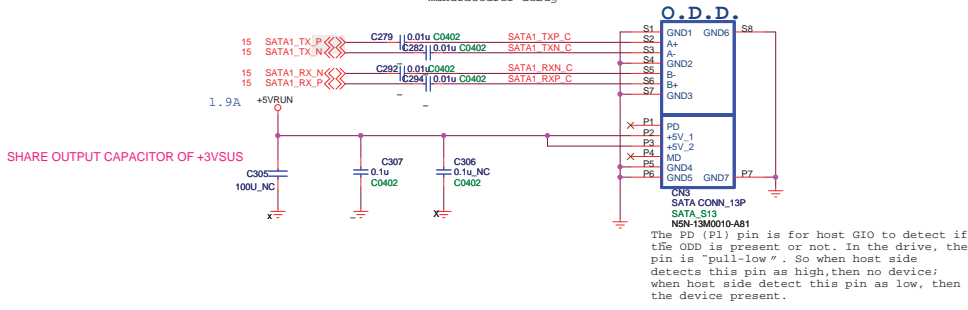






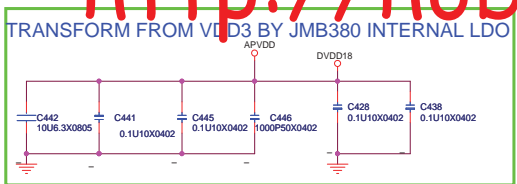
### SATA DVD

The MD (P4) pin is for ODD PN & FOOTPRINT N/A  
manufacturer debug

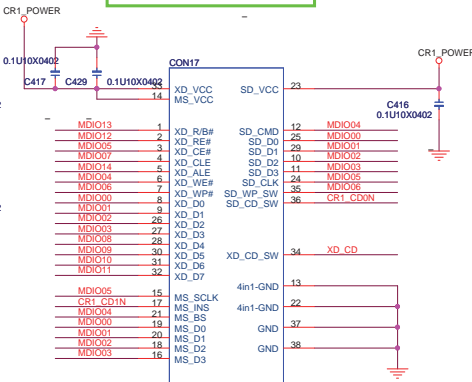
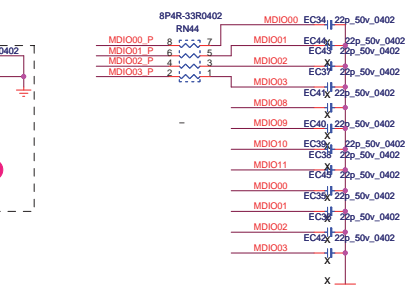
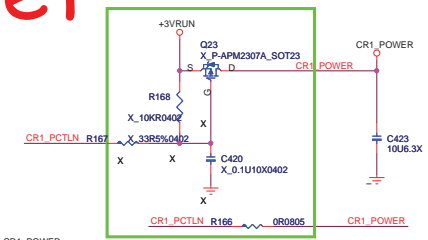
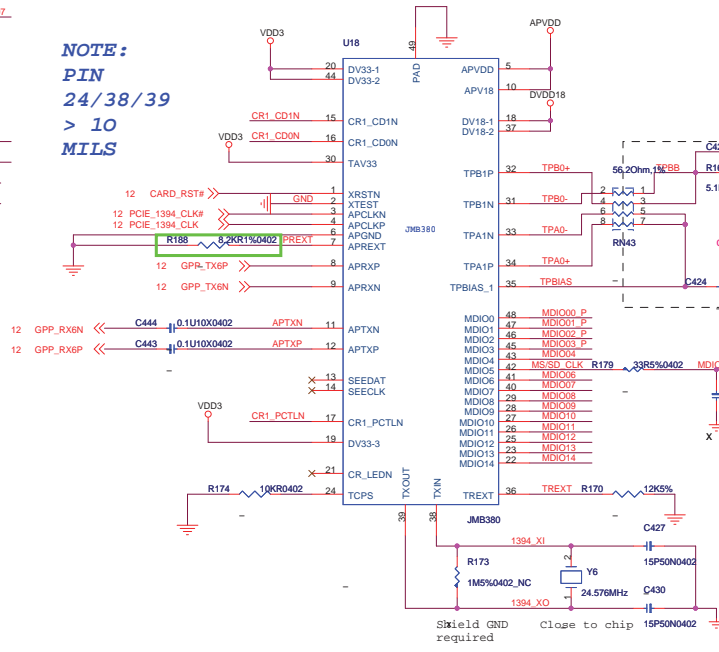




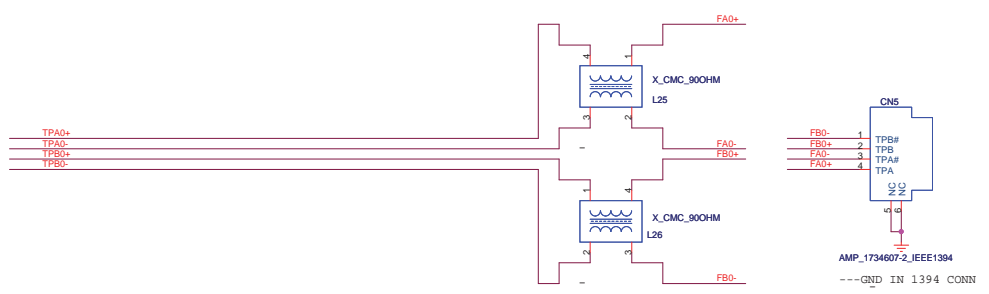


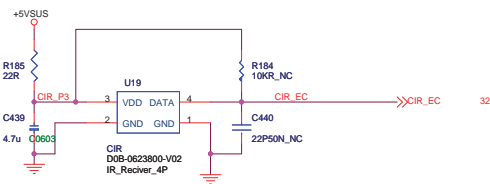
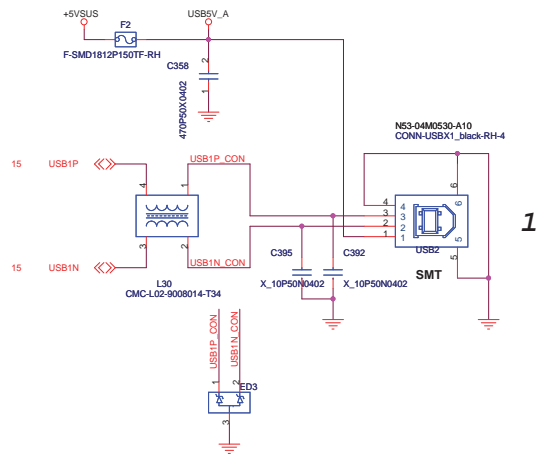
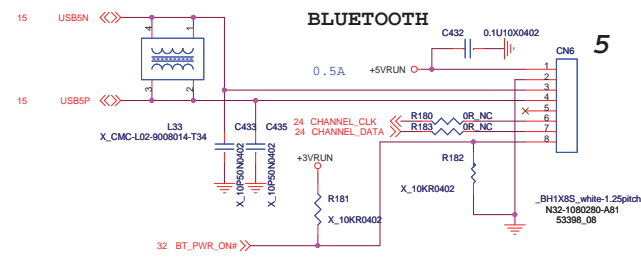
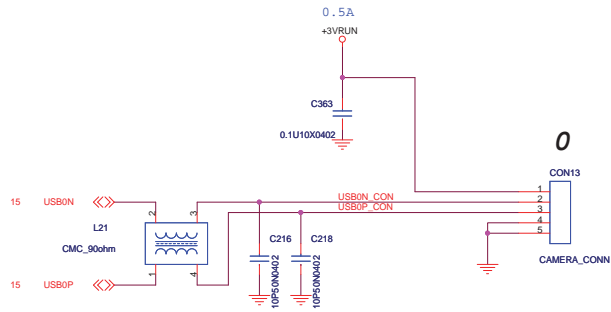


**NOTE:**  
PIN  
24/38/39  
> 10  
MILS



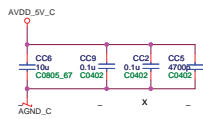
Media I/F	SD Card	Memory Stick	xD Card
MDIO00	SD_DATA0	MS_DATA0	XD_DATA0
MDIO01	SD_DATA1	MS_DATA1	XD_DATA1
MDIO02	SD_DATA2	MS_DATA2	XD_DATA2
MDIO03	SD_DATA3	MS_DATA3	XD_DATA3
MDIO04	SD_CMD	MS_BS	XD_WE#
MDIO05	SD_CLK	MS_CLK	XD_CE#
MDIO06	SD_WP	X	XD_WP#
MDIO07	X	X	XD_CLE
MDIO08	X	X	XD_DATA4
MDIO09	X	X	XD_DATA5
MDIO10	X	X	XD_DATA6
MDIO11	X	X	XD_DATA7
MDIO12	X	X	XD_RE#
MDIO13	X	X	XD_R/#
MDIO14	X	X	XD_ALE
CR1_CDIN	X	MS_INS	X
CR1_CDON	SD_CD	X	X



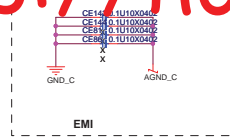
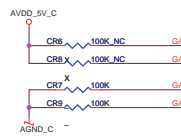




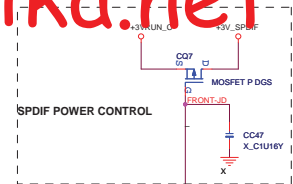




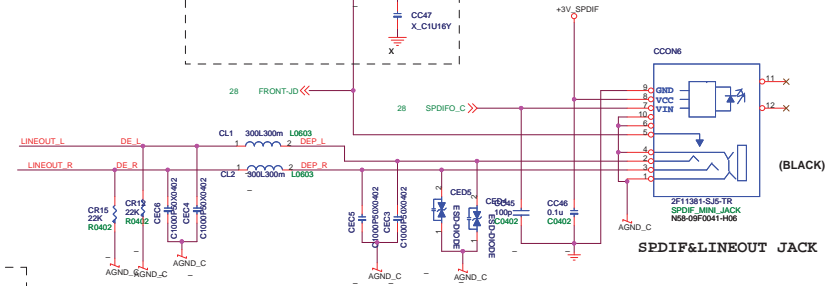
	GAIN0	GAIN1	SE/BTLF
6dB	0	0	0
10dB	0	1	0
15.6dB	1	0	0
21.6dB	1	1	0
4.3dB	X	X	1



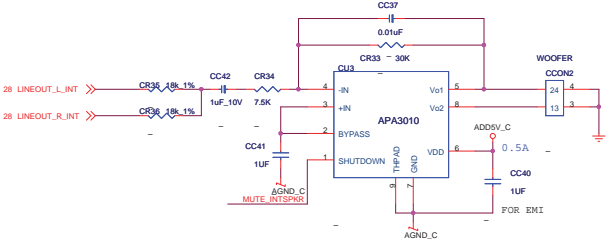
EMI



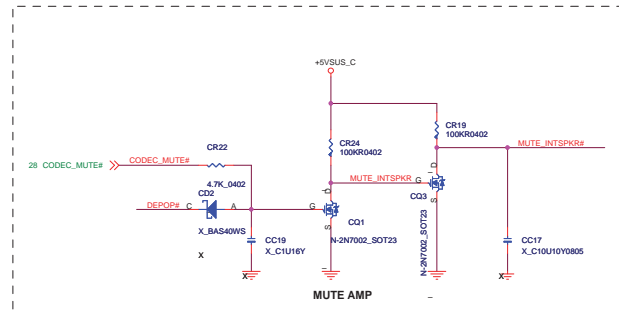
SPDIF POWER CONTROL



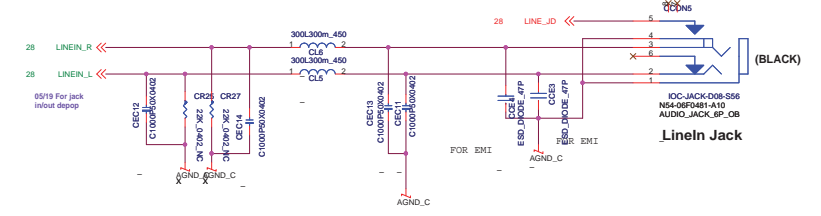
SPDIF & LINEOUT JACK



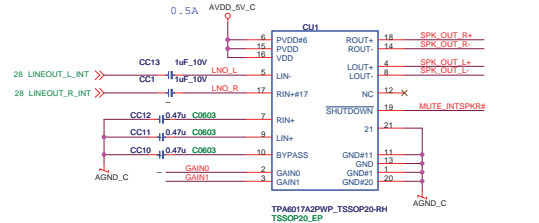
Internal Woofer Amp & Connector



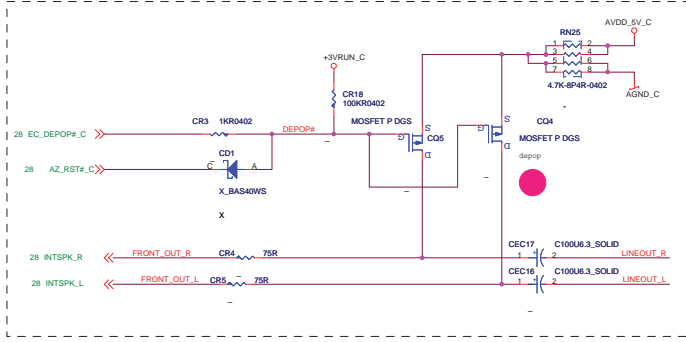
MUTE AMP



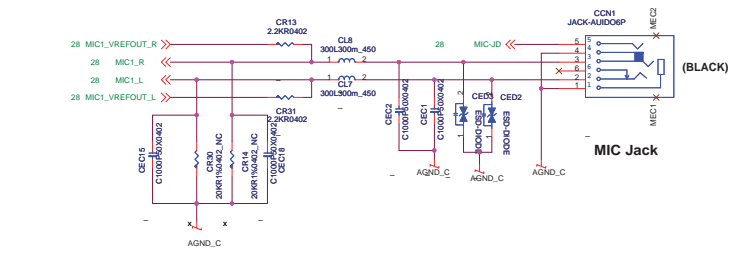
LineIn Jack



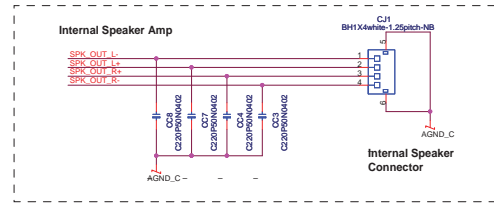
TPA6017A2PWP\_TSSOP20-RH TSSOP20\_EP



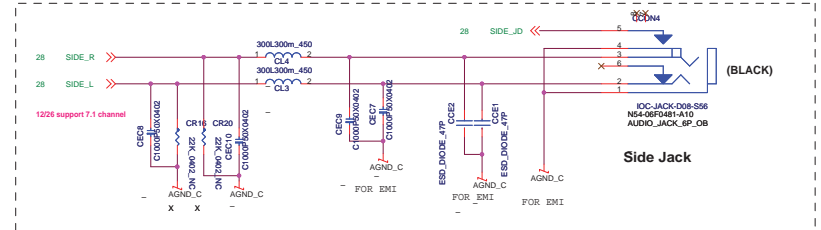
POWER ON/OFF/S3/S4 NOISE CONTROL



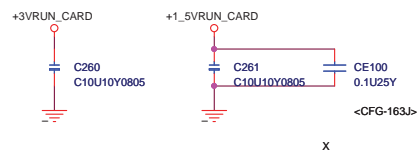
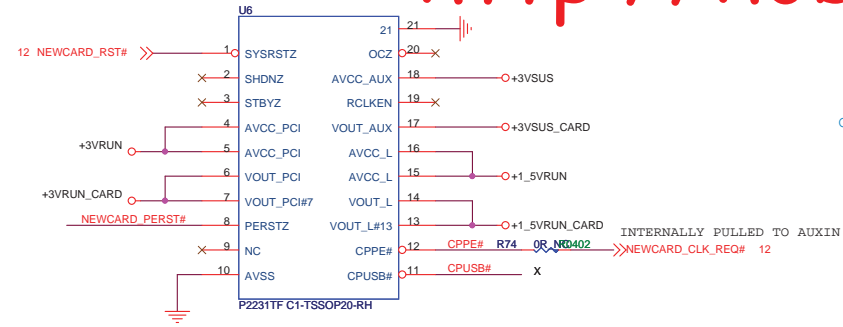
MIC Jack



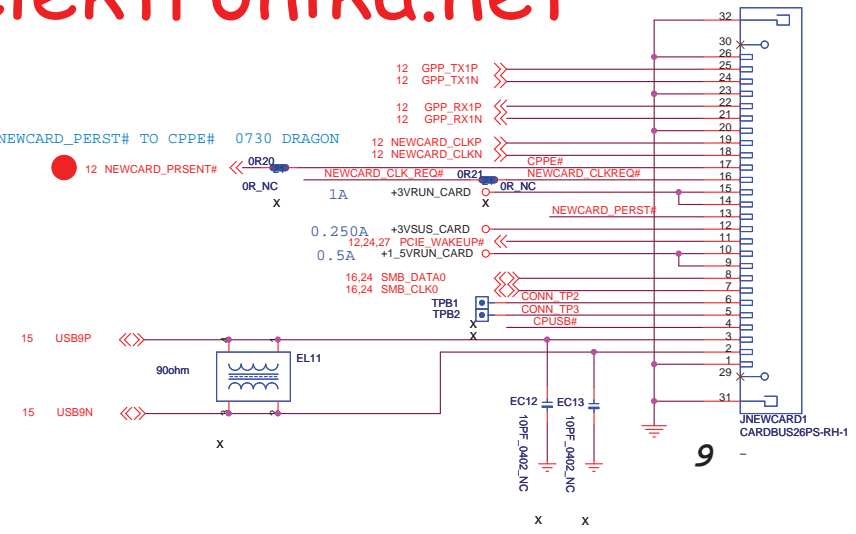
Internal Speaker Connector



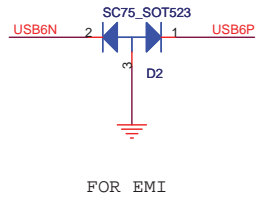
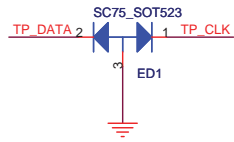
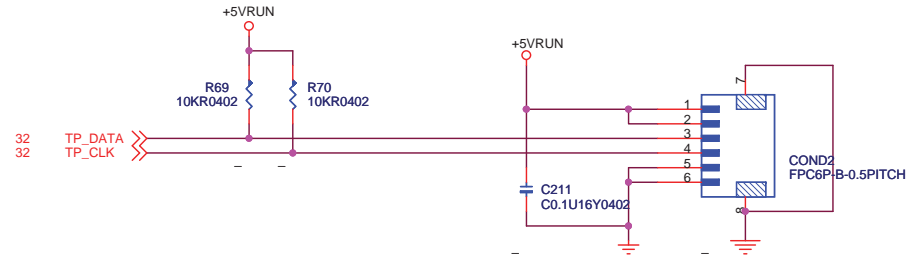
Side Jack



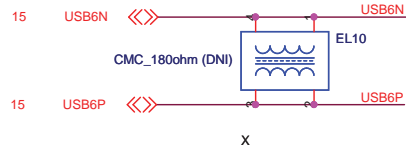
CHANGED FROM NEWCARD\_PERST# TO CPPE# 0730 DRAGON



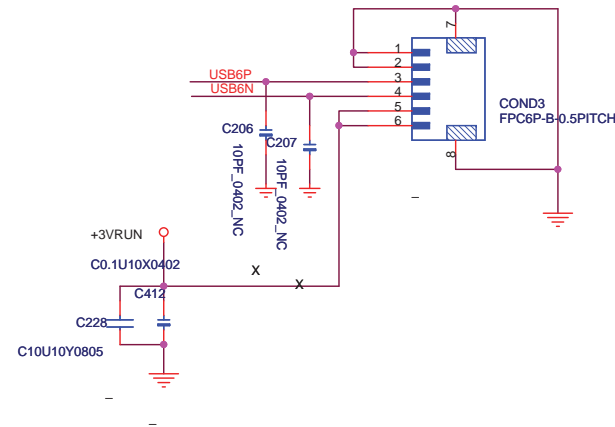
### TOUCH PAD




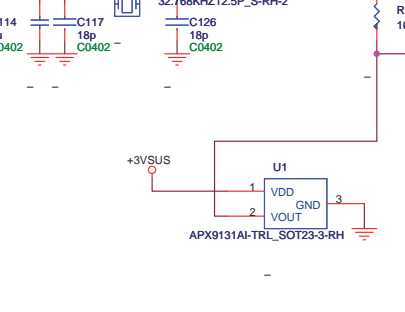
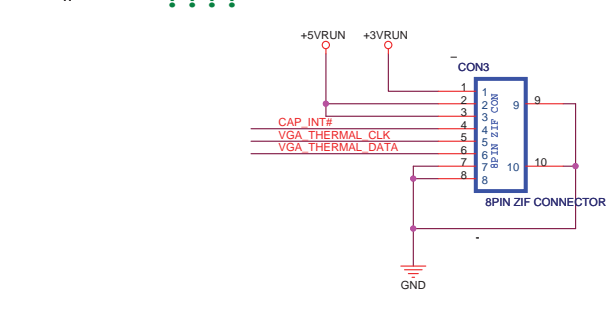
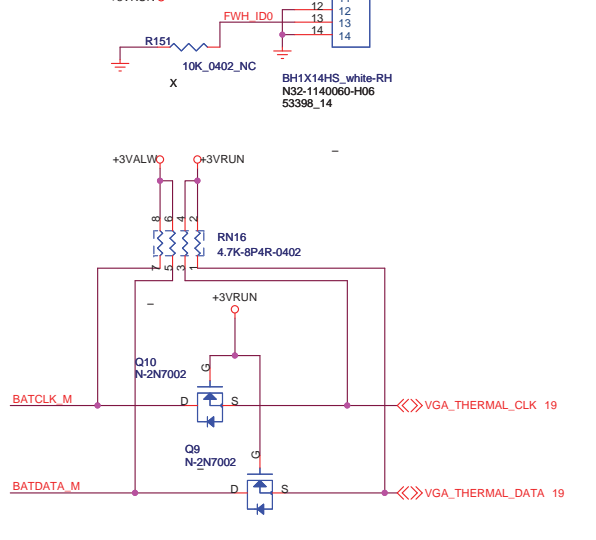
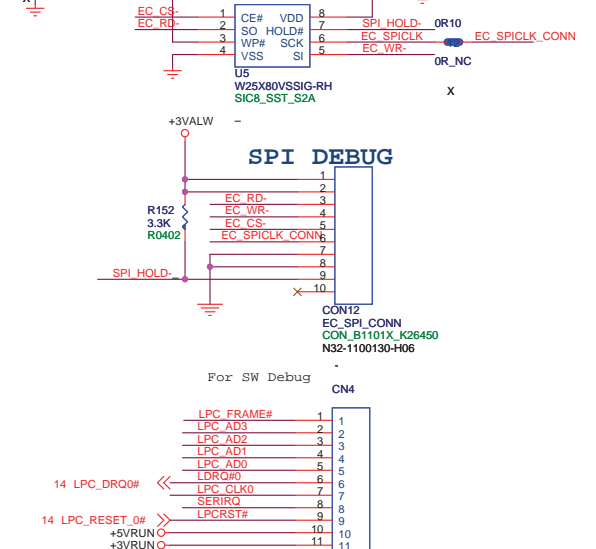
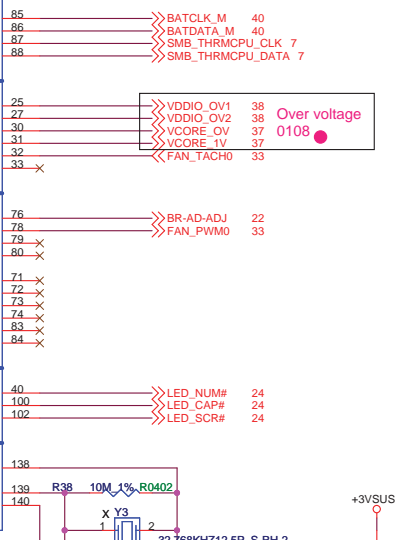
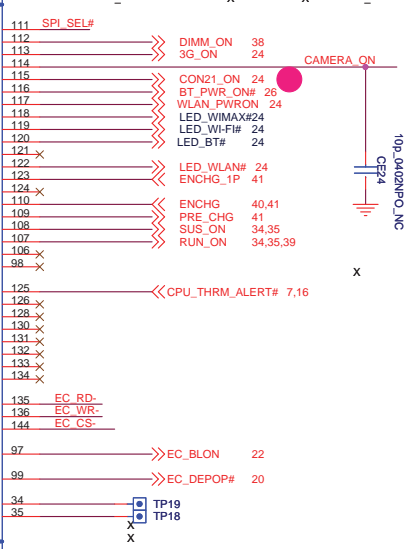
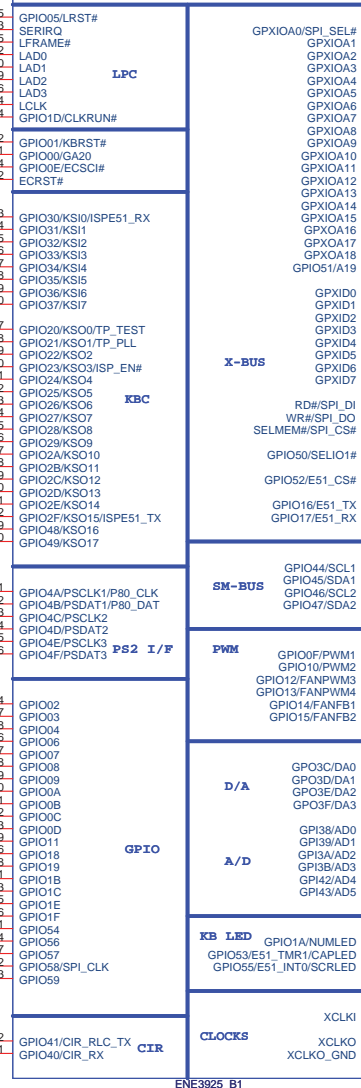
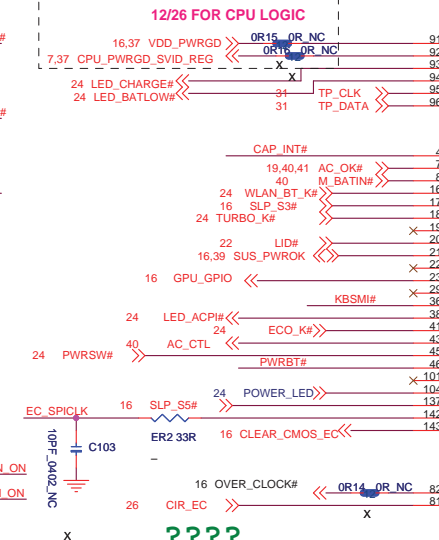
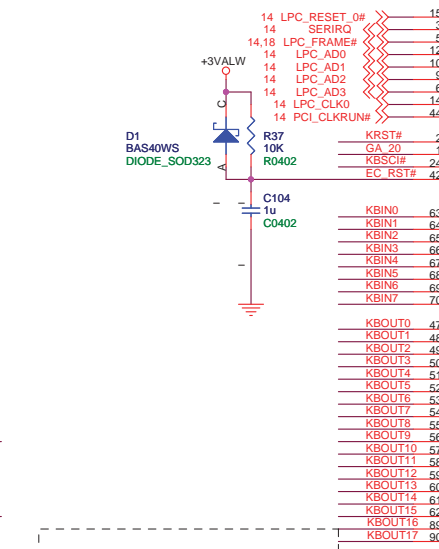
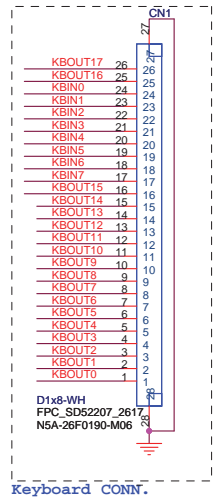
FOR EMI



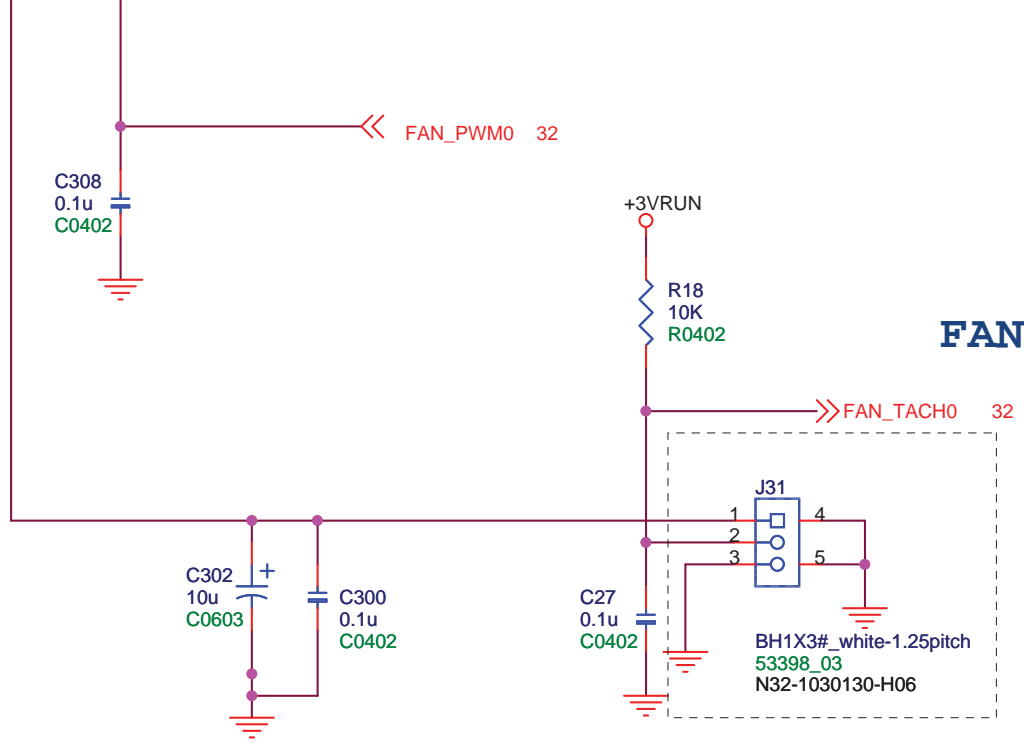
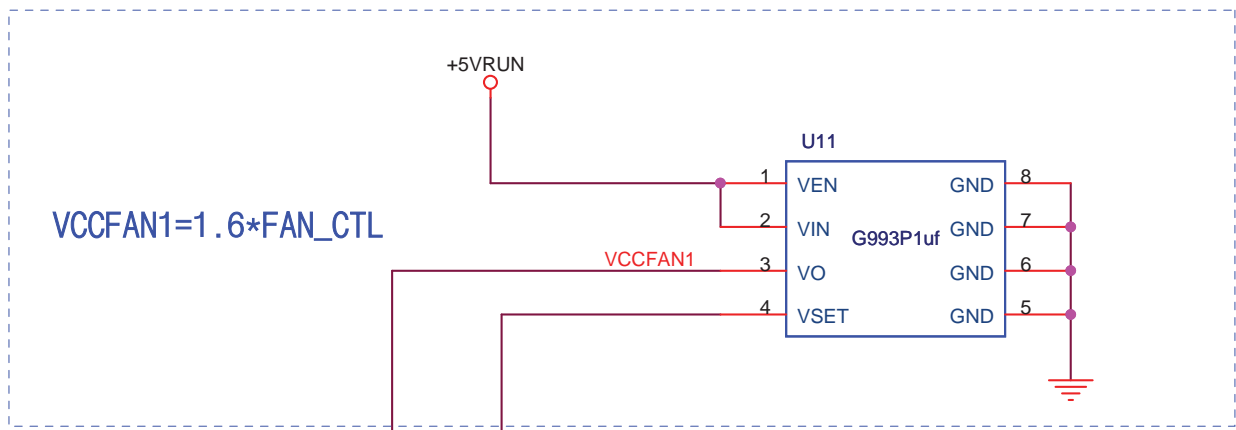
### FINGERPRINT




 <b>MICRO-STAR INT'L CO.,LTD.</b>	
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<b>TPM</b>	
Size	Document Number
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 **MICRO-STAR INT'L CO.,LTD.**

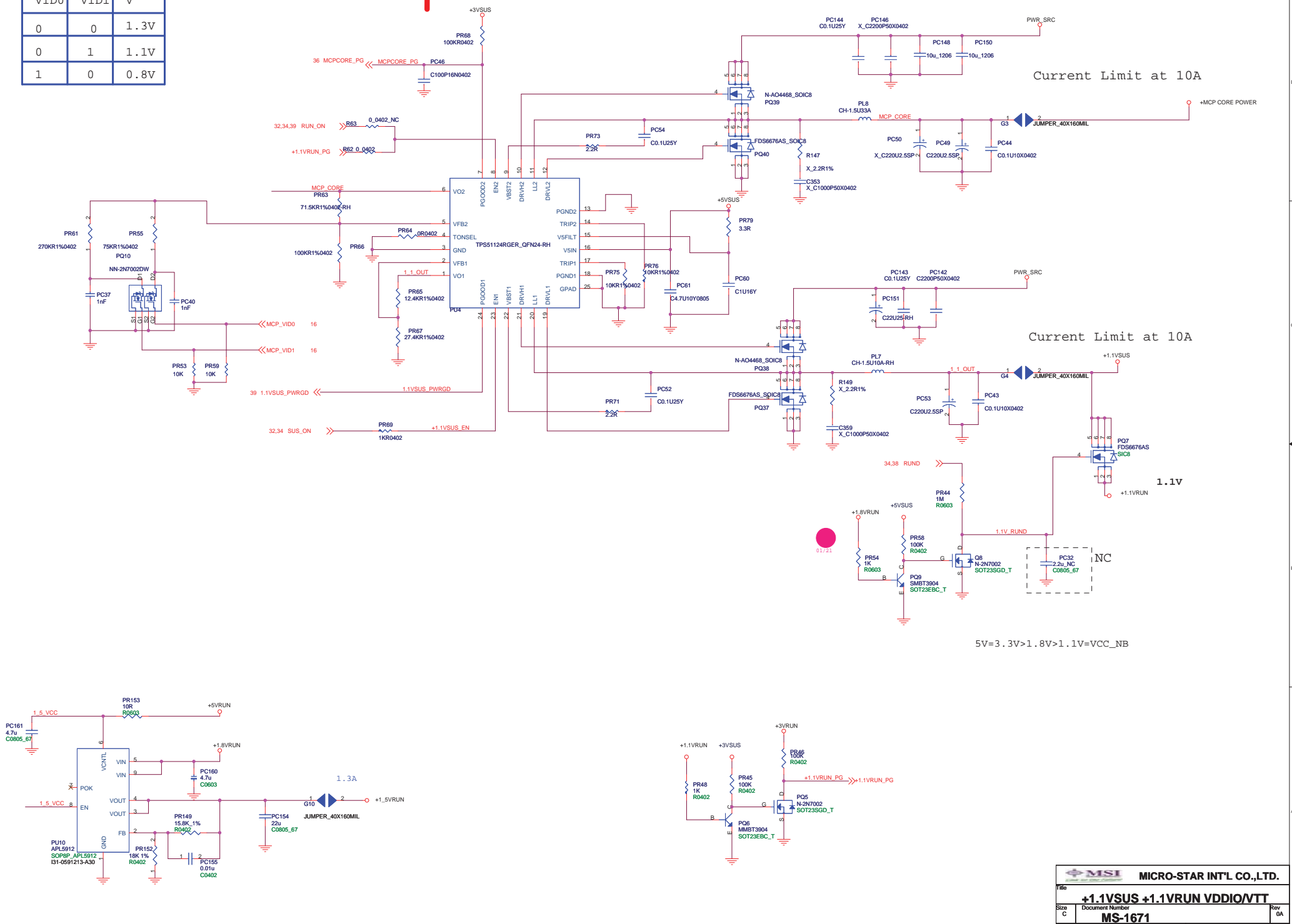
Title  
**SYA FAN**

Size A	Document Number <b>MS-1671</b>	Rev 0A
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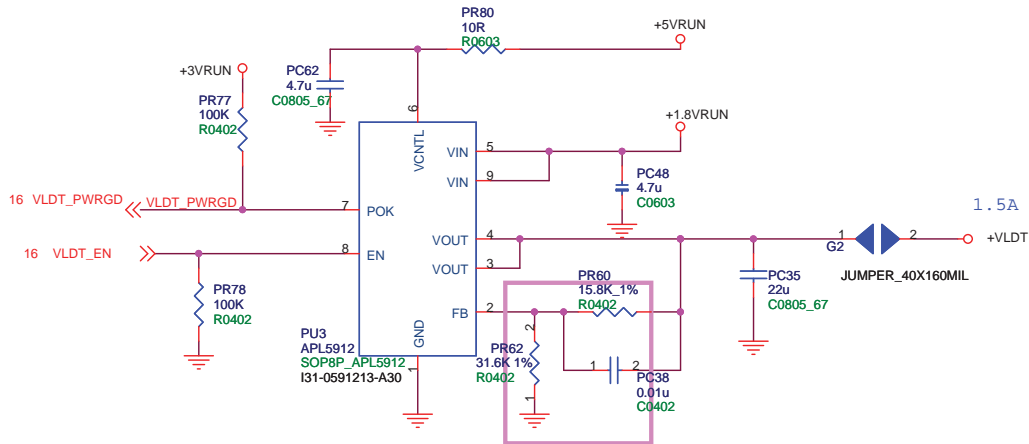
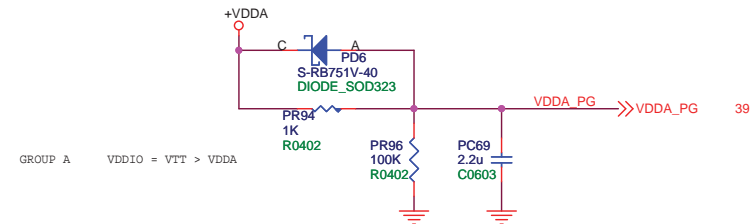
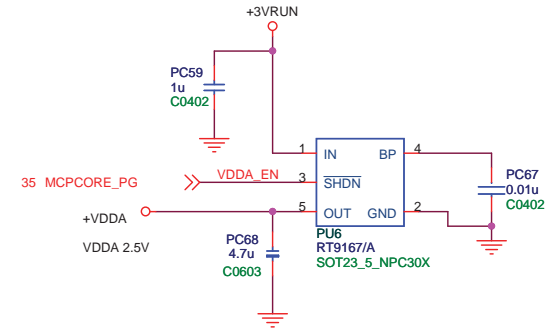
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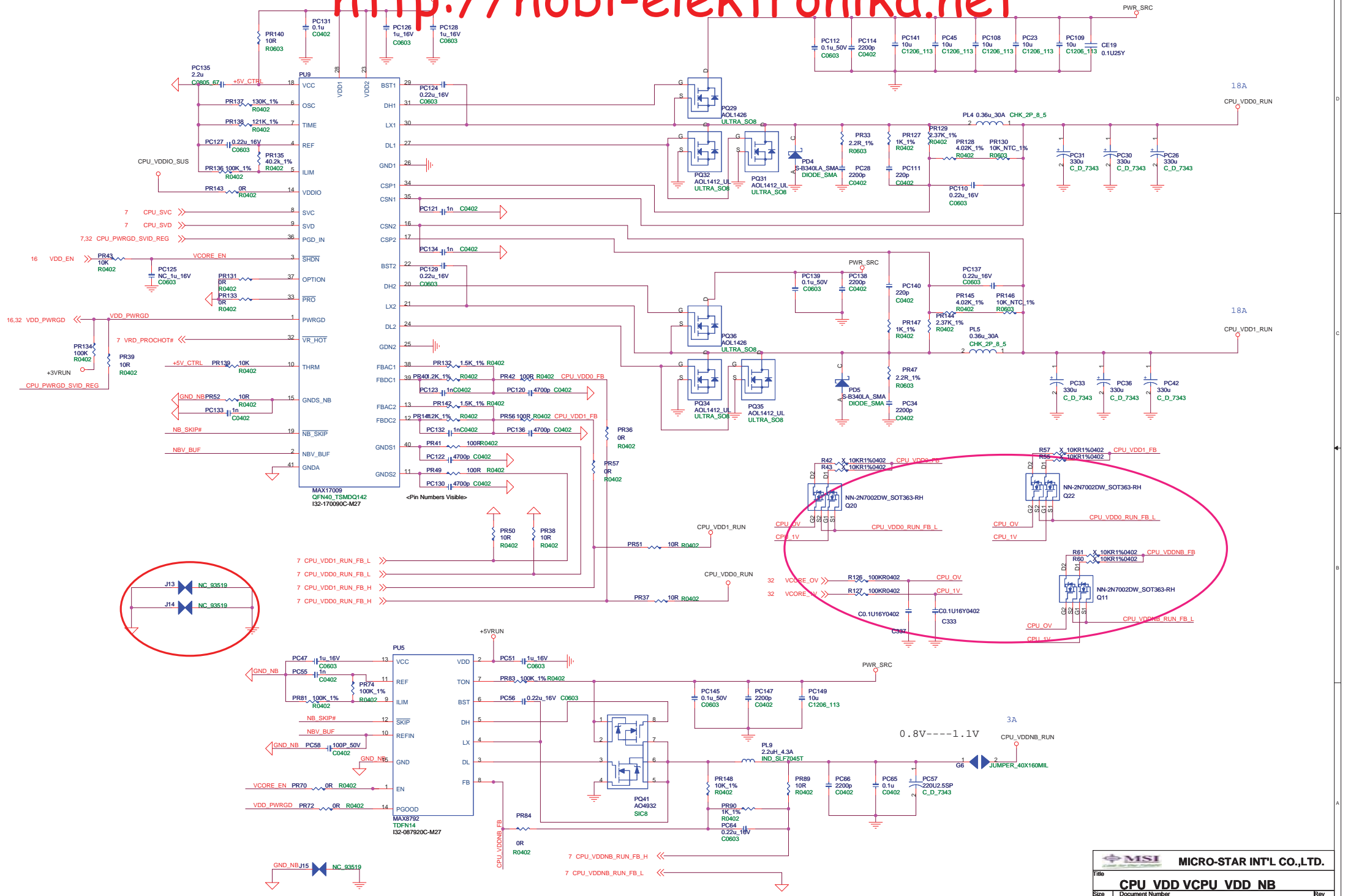
VID0	VID1	V
0	0	1.3V
0	1	1.1V
1	0	0.8V



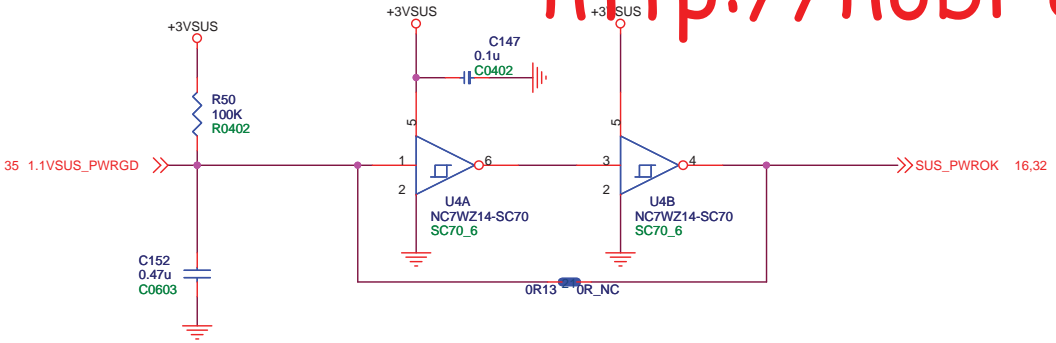
1.8VRUN>1.2VRUN>1.1VRUN



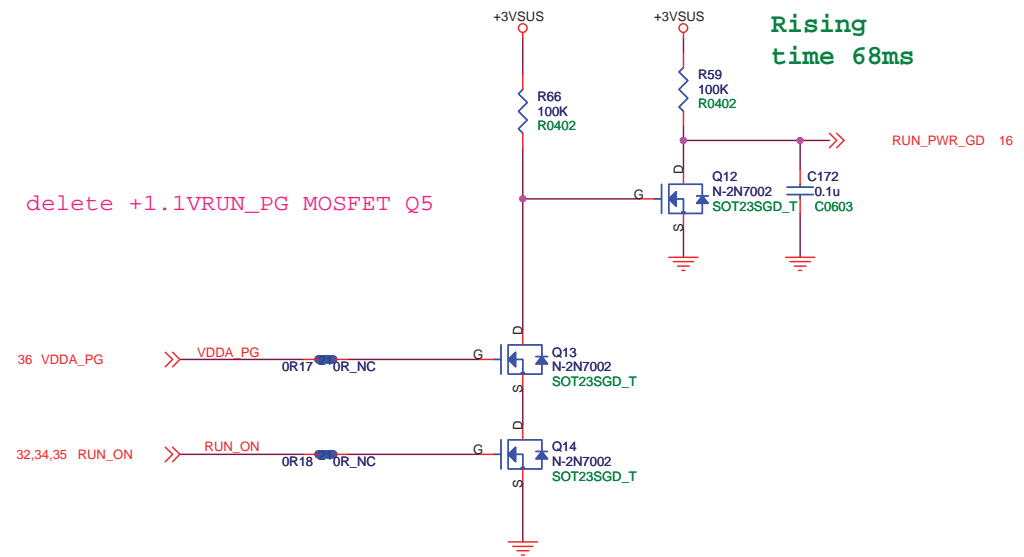
 <b>MICRO-STAR INT'L CO.,LTD.</b>	
Title	
<b>VDDA VLDT +2.5VRUN</b>	
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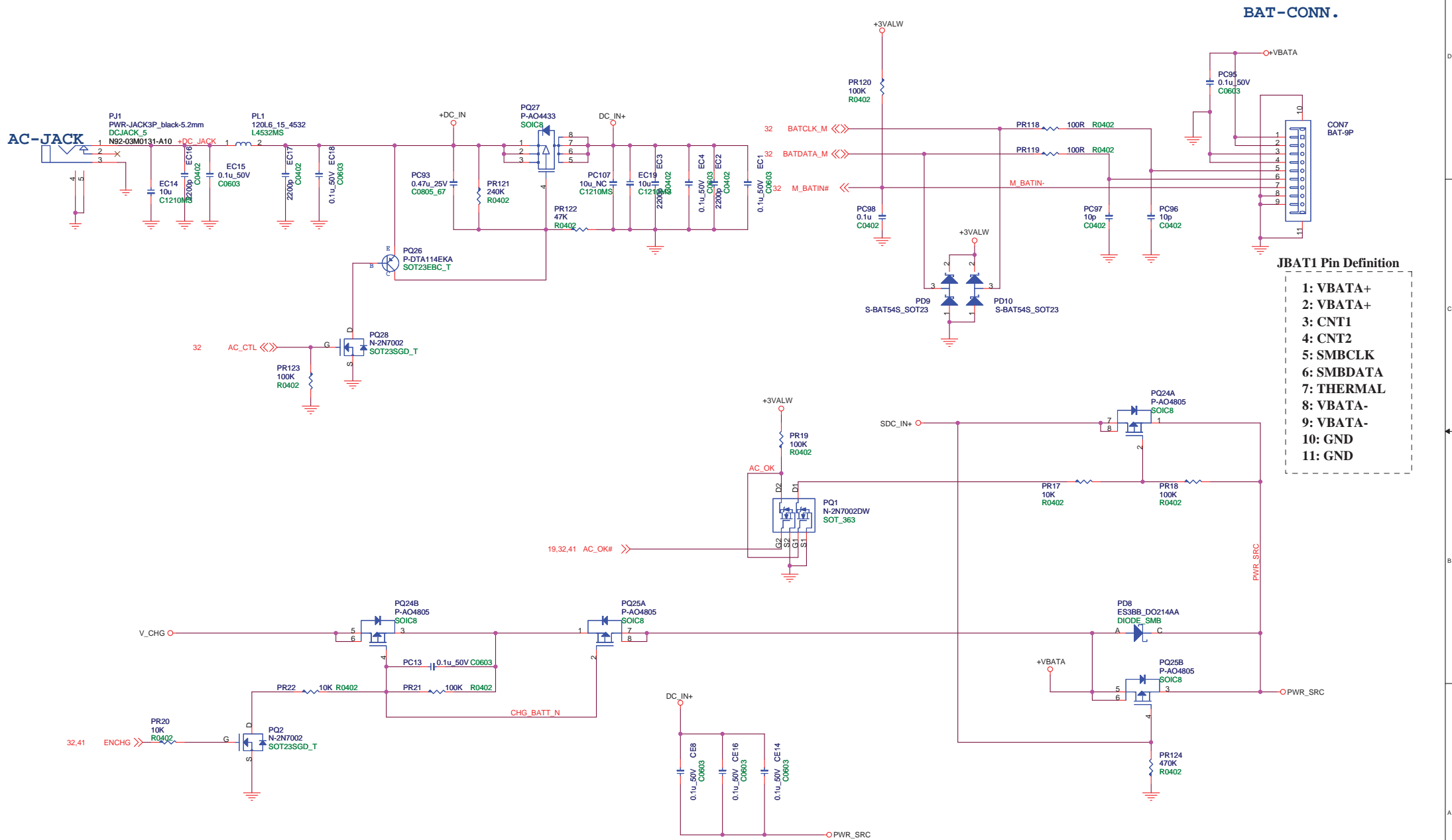


delete +1.1VRUN\_PG MOSFET Q5



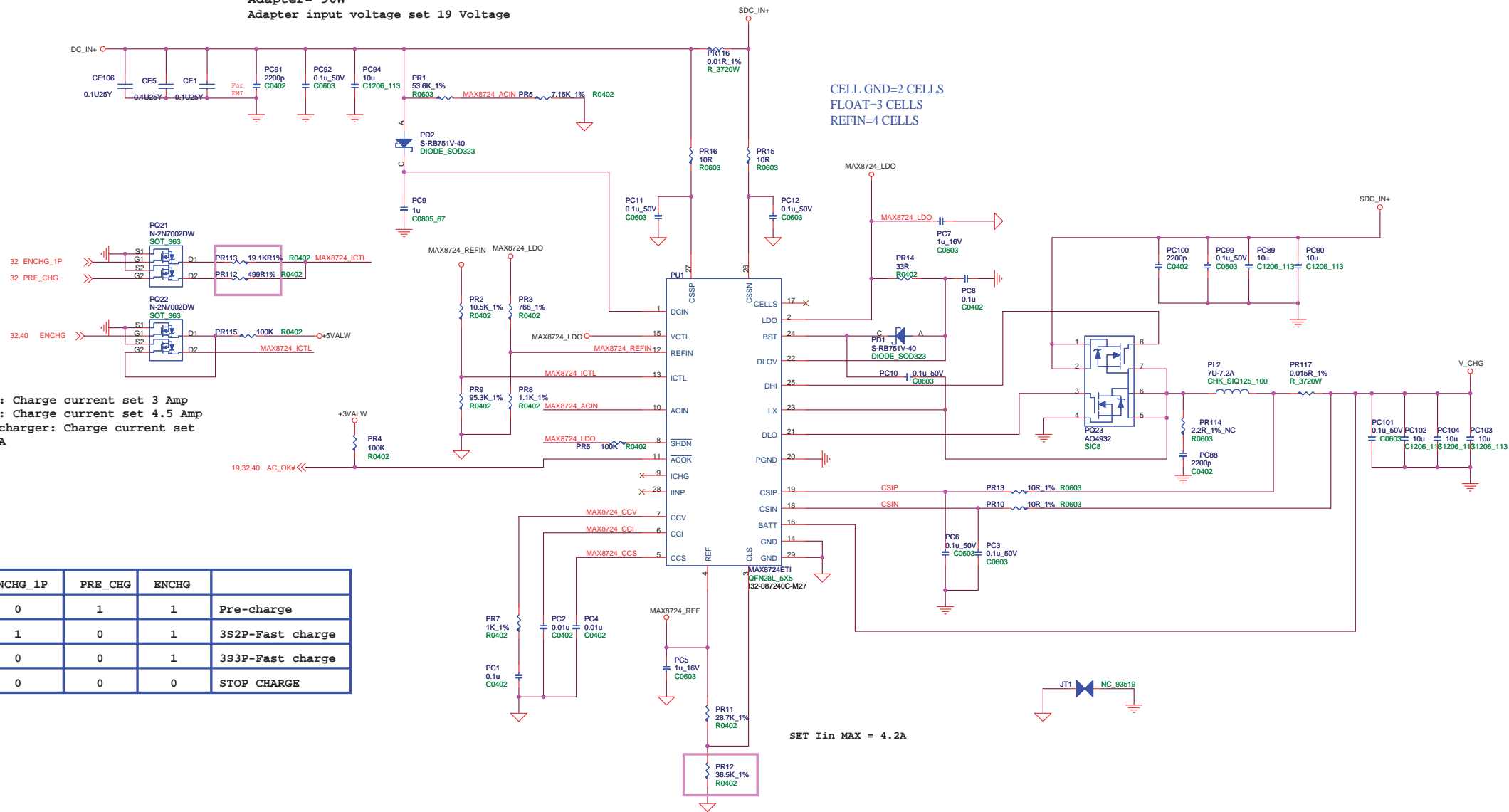
Rising time 68ms

 MICRO-STAR INT'L CO.,LTD.	
Title	
<b>POWER GOOD</b>	
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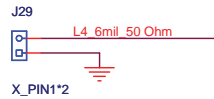
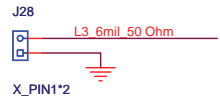




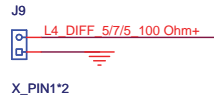
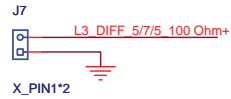
Adapter= 90W  
Adapter input voltage set 19 Voltage



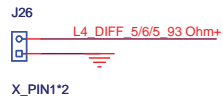
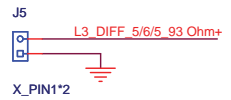
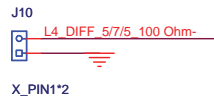
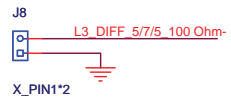
ENCHG_1P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	3S2P-Fast charge
0	0	1	3S3P-Fast charge
0	0	0	STOP CHARGE



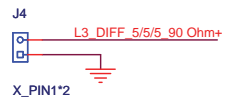
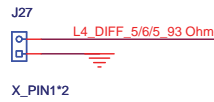
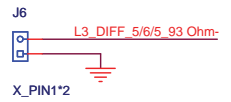
RGB Signal 50 Ohm



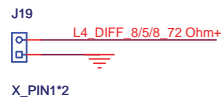
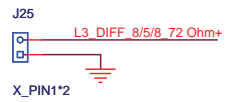
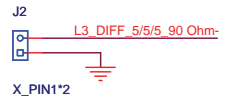
Differential Pair 100 Ohm



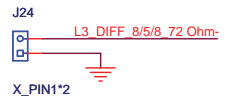
Differential Pair 93 Ohm




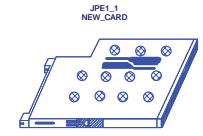
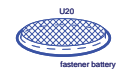
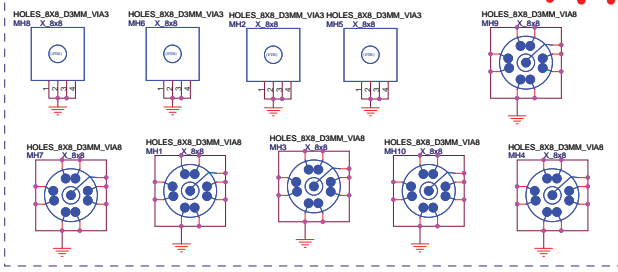
Differential Pair 90 Ohm



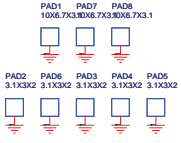
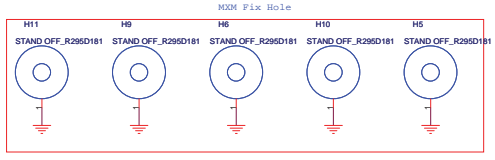
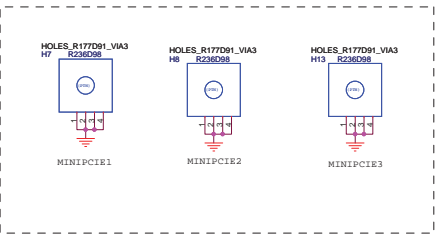
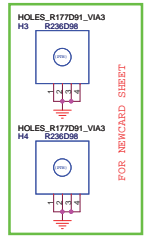
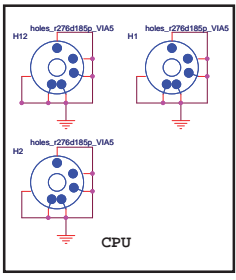
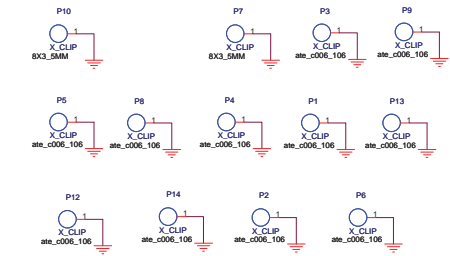
Differential Pair 72 Ohm



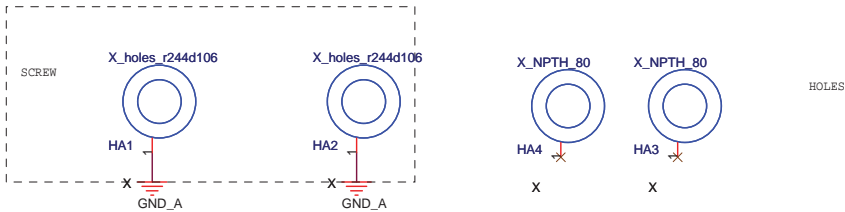
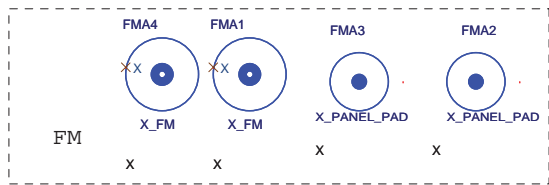
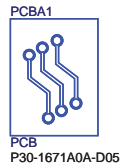
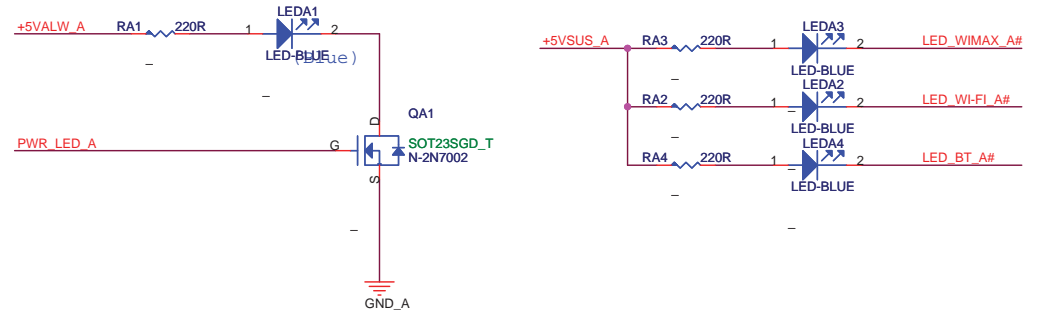
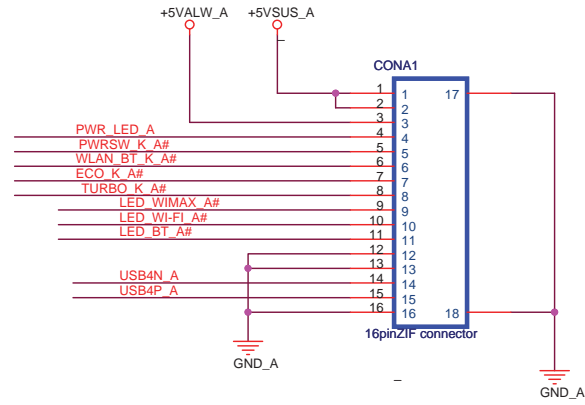
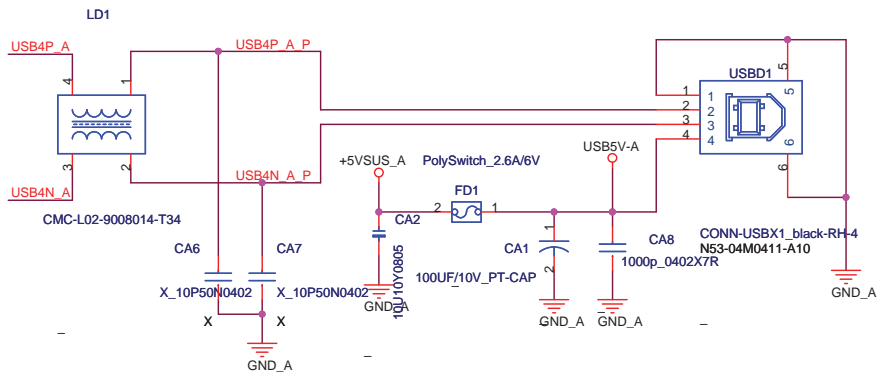
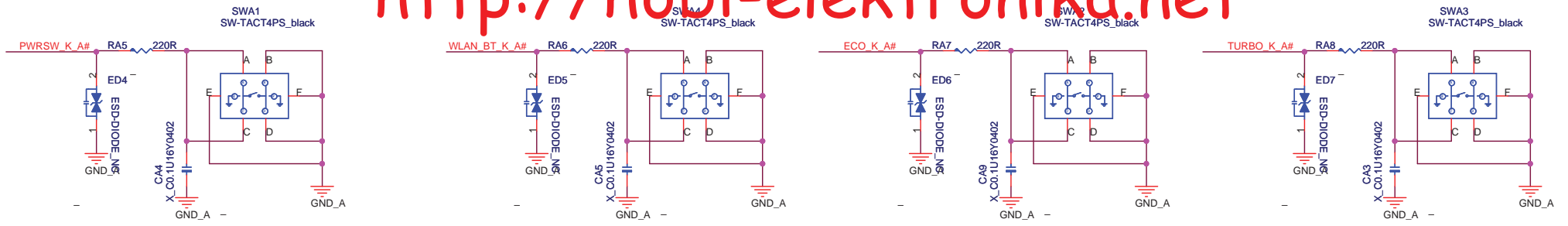
 <b>MICRO-STAR INT'L CO.,LTD.</b>	
Title	
<b>PCB IMPEDANCE JUMP</b>	
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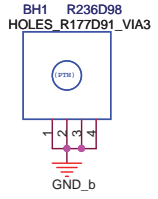
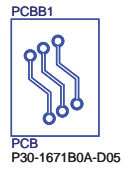
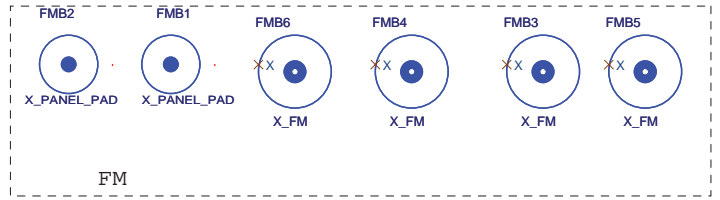
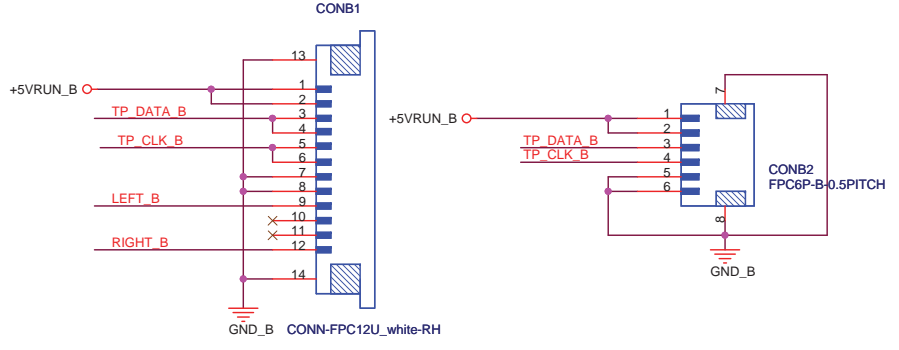
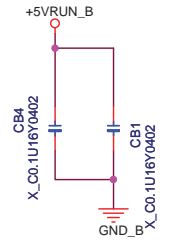
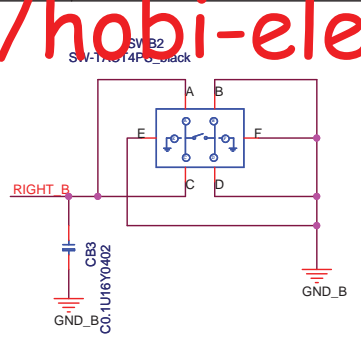
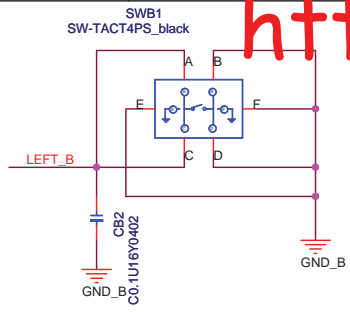
PCI EXPRESS  
SHIELDING :  
E2M-221011-SH4



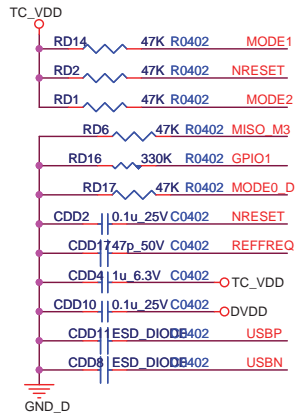




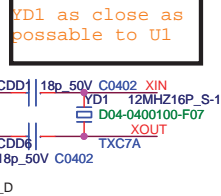
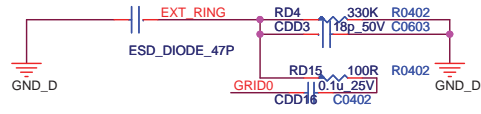
<b>MICRO-STAR INT'L CO.,LTD.</b>	
Title <b>LANUCH BOARD</b>	
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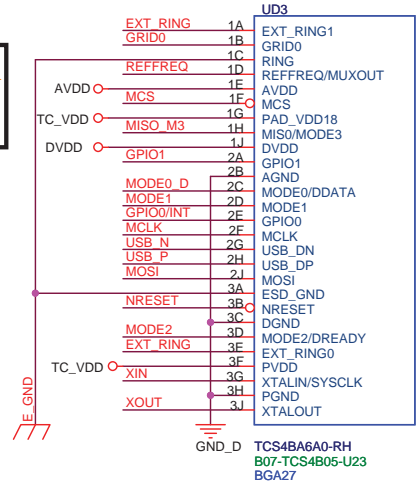
<b>MICRO-STAR INT'L CO.,LTD.</b>		
Title <b>TOUCH PAD</b>		
Size B	Document Number <b>MS-1671B</b>	Rev 0A
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change GND to pin CDD6 and GPIO/INT 02/13

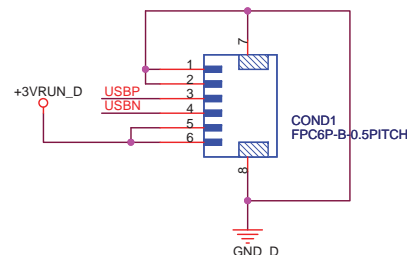
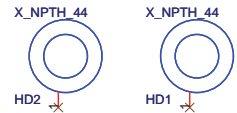
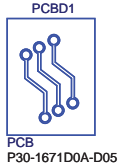
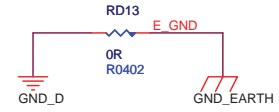
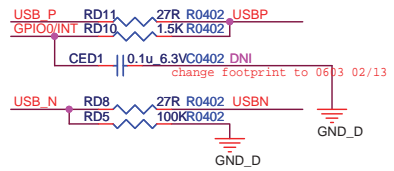
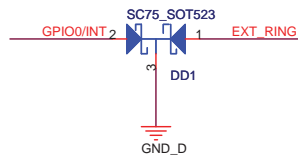
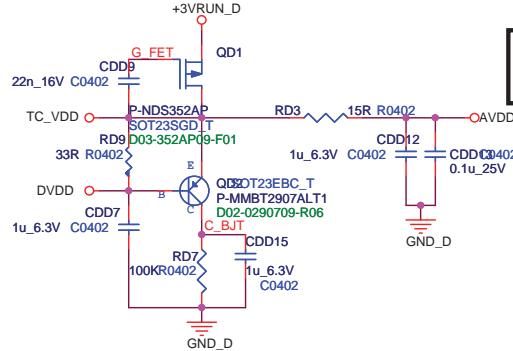
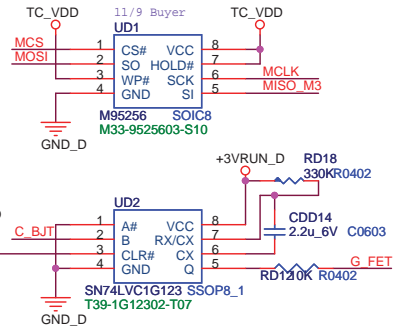


keep the trace EXT\_RING width 10mil and as short as possible



E\_GND layout on surface layer

clear 10mil space around U1



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P12 Add R9 11/9

P14 Change R184 R175 from 220hm to 120hm 11/9

P15 Add USB pull low R 11/9

P16 Remove R42 11/9

P19 Add R8 11/9

P22 Add R6 11/9

P32 Add R253 11/9

P46 Swap LAN conn pin diefine 11/10


P34-38 change power from Allen 11/13

P32 change ps2 port3 as tp interface 11/13

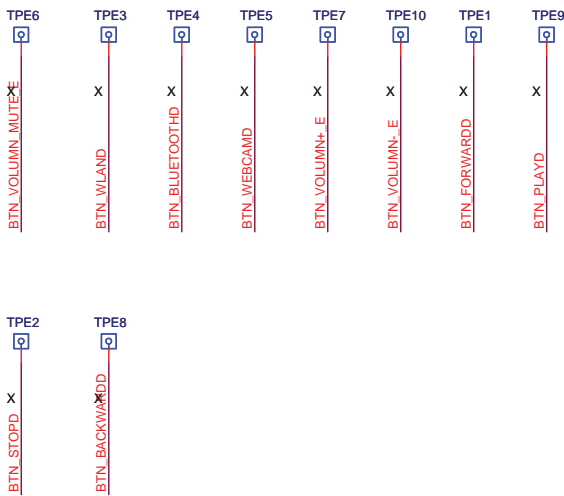
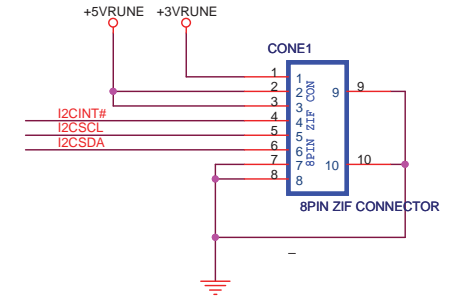
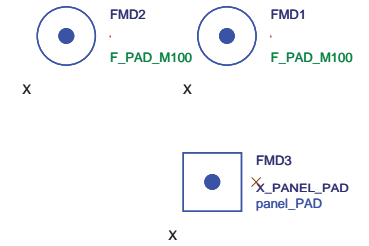
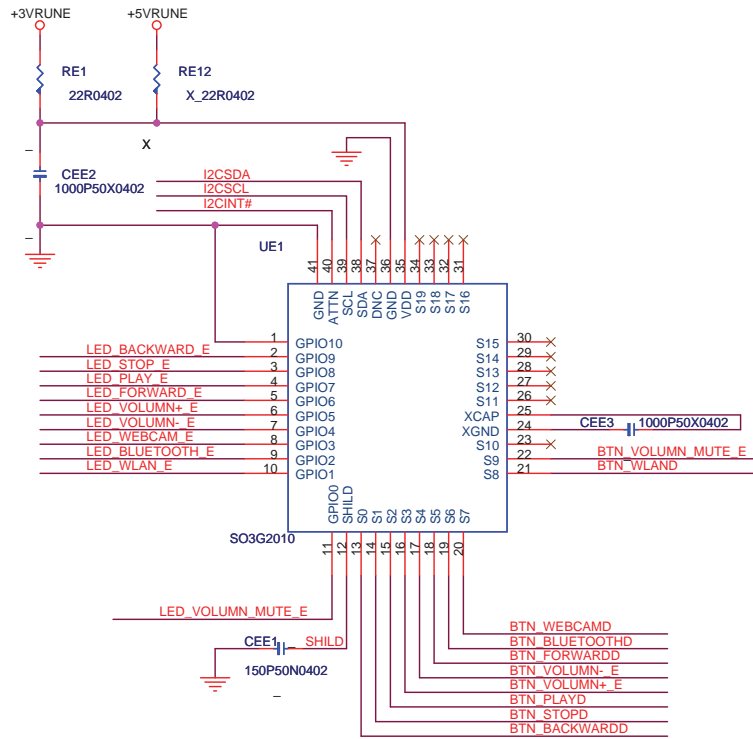
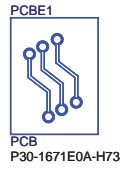
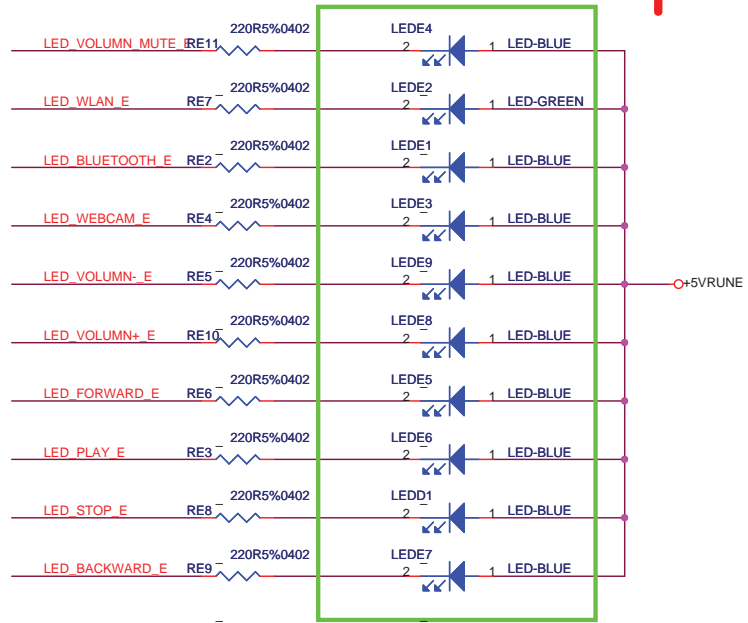
P20 del switch and 0ohm 11/16

P29 add 2 pin mic connector for channel 11/22

P25 CHANG SUS POWER TO RUN POWER 11/27

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