1215 SCHEMATIC Revision1.1

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27	PCH_IBEX(8)_POWER,GND
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91	POWER_LOAD SWITCH
92	POWER_FLOWCHART
95	POWER_Latch

<Variant Name>

ASUSTeK COMPUTER INC

Title : PAGE REF.

Engineer: Aries/Jesse

Size	Project Name	Rev
Custom	1215	1.0

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SYSTEM PAGE REF.

PAGE	Content
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7	DIM-DDR3 SO-DIMM CHANNEL A
8	DIM-DDR3 SO-DIMM CHANNEL B
9	DIM-DDR3 VREF & TERMINATION
20	PCH_IBEX(1)SATA,IHDA,RTC,LPC
21	PCH_IBEX(2)_PCIE,CLK,SMB,PEG
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27	PCH_IBEX(8)_POWER,GND
28	PCH_SPI ROM,OTH
29	CLK_ ICS9LPRS427CGLFT
30	EC_ KB3310QF
31	KB
42	CARD READER AU6433
44	BUG-DEBUG PORT
45	HDMI CONN
46	CRT-LVDS CONN
47	CRT-D-SUB CONN
50	FAN-THERMAL SENSOR, FAN CONN
51	XDD-SATA HDD CONN
52	USB-USB 2.0 CONN*1
53	MINI-PCIE WLAN CONN
56	LED- PWR,LED,FPC CONN
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60	DC_-DC, BATT CONN
61	BT_-BLUETOOTH CONN
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65	ME_-SCREW HOLE, SMT NUT
66	RTC_DC CON
67	CMO-CMOS CAMERA
68	Board to Board CONN
69	OTH-EXPRESS GATE
70	VGA_nVIDIA_N11M-GE2_PCIE
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72	VGA_nVIDIA_N11M-GE2_Display
73	VGA_nVIDIA_N11M-GE2_XTAL
74	VGA_nVIDIA_N11M-GE2_GPIO
75	GA_nVIDIA_N11M_40nm_DDR3
76	GA-Power
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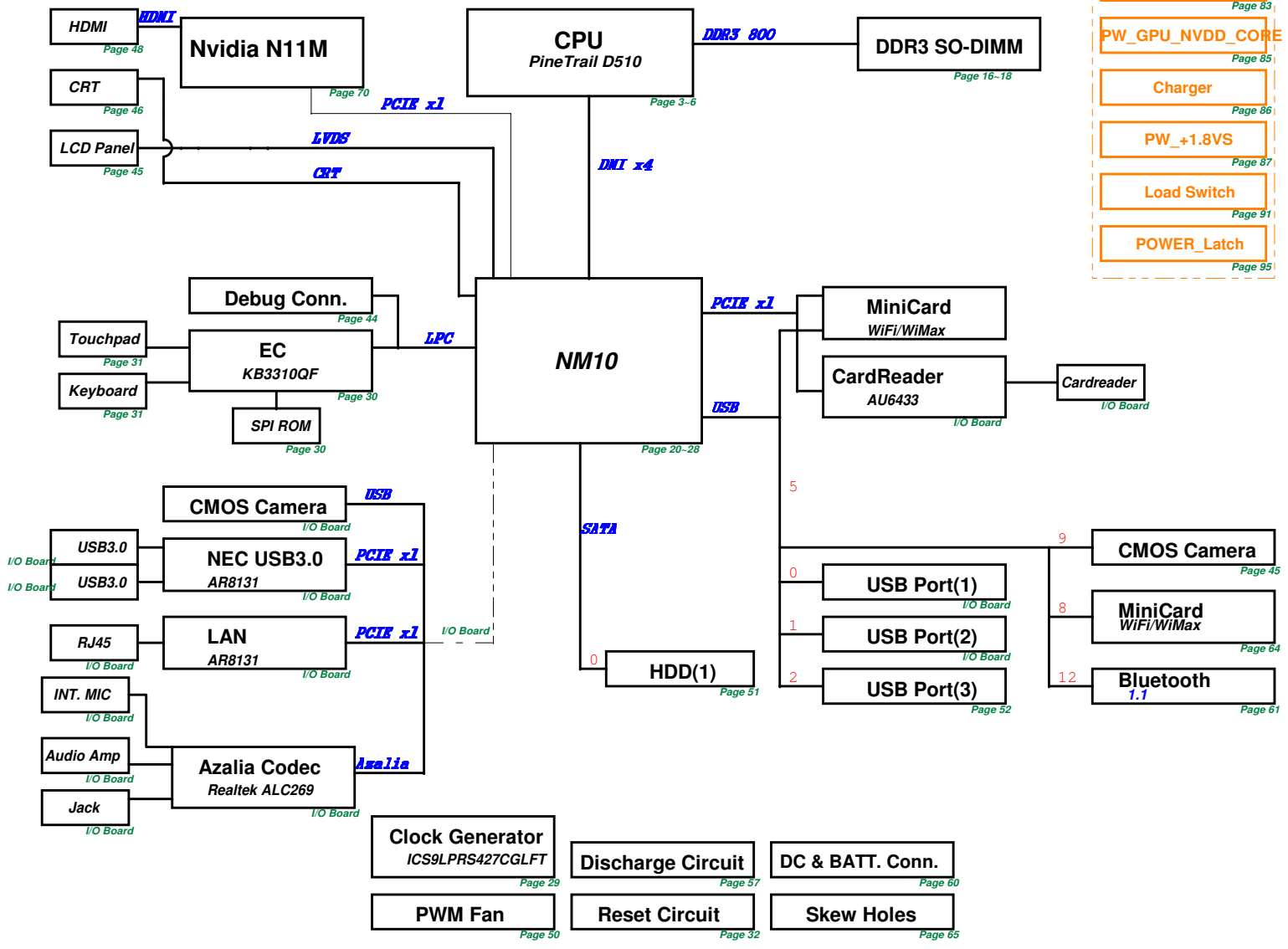
97	Power On Sequence
80	W_VCORE(RT8152D)
81	PW_SYSTEM(RT8205C)
82	PW_I/O_VCCP(RT8202A)
83	PW_I/O_DDR(RT8202A+uP7711)
85	PW_GPU_NVDD_CORE(RT8202A)
87	PW_+1.8VS
88	POWER_CHARGER
91	POWER_LOAD SWITCH
92	POWER_FLOWCHART
95	POWER_Latch

1215N SCHEMATIC Revision 1.00

BLOCK DIAGRAM



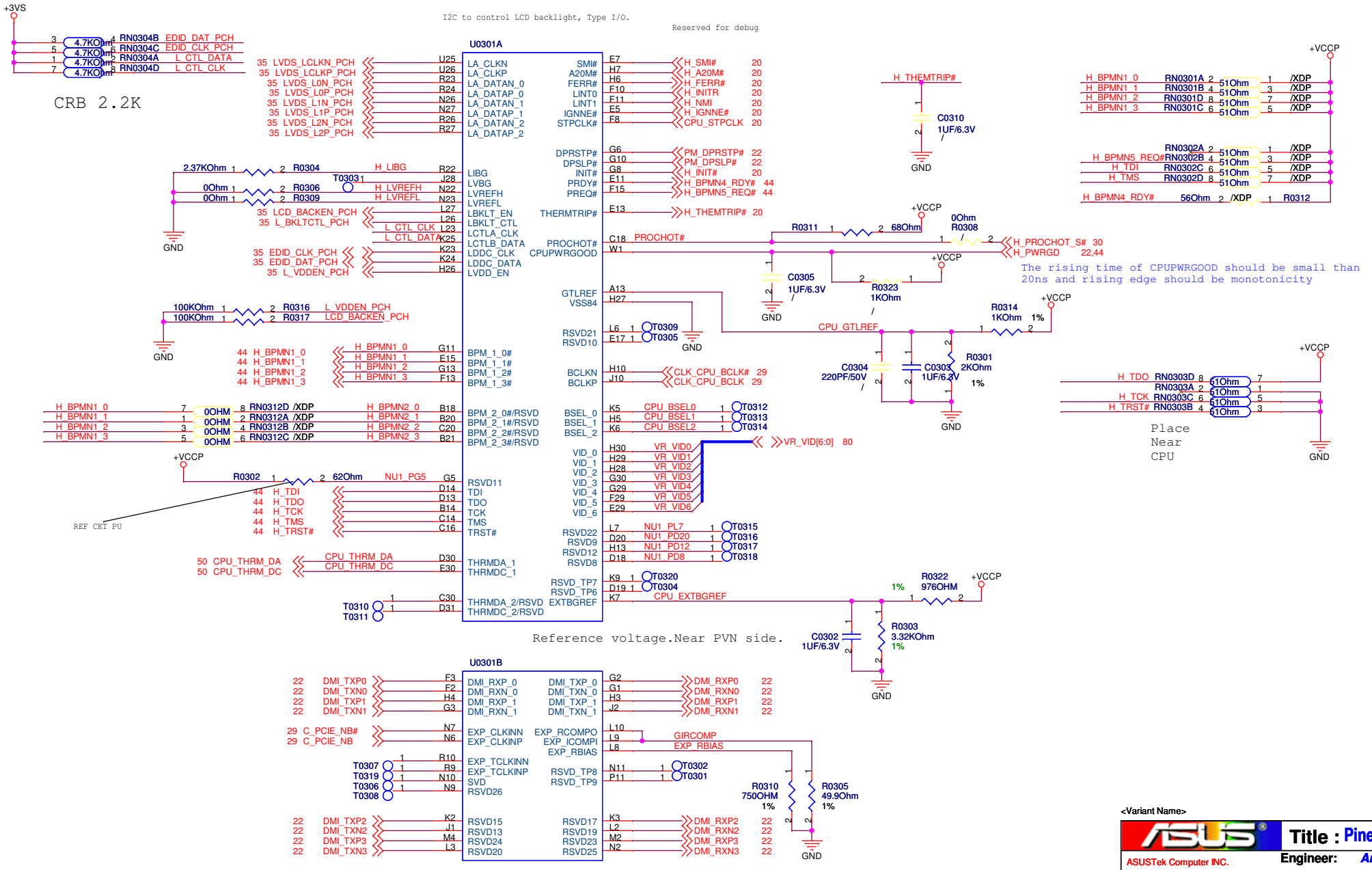
ASUSTeK COMPUTER INC. NB4

Title : Block Diagram

Engineer: Aries/Jesse

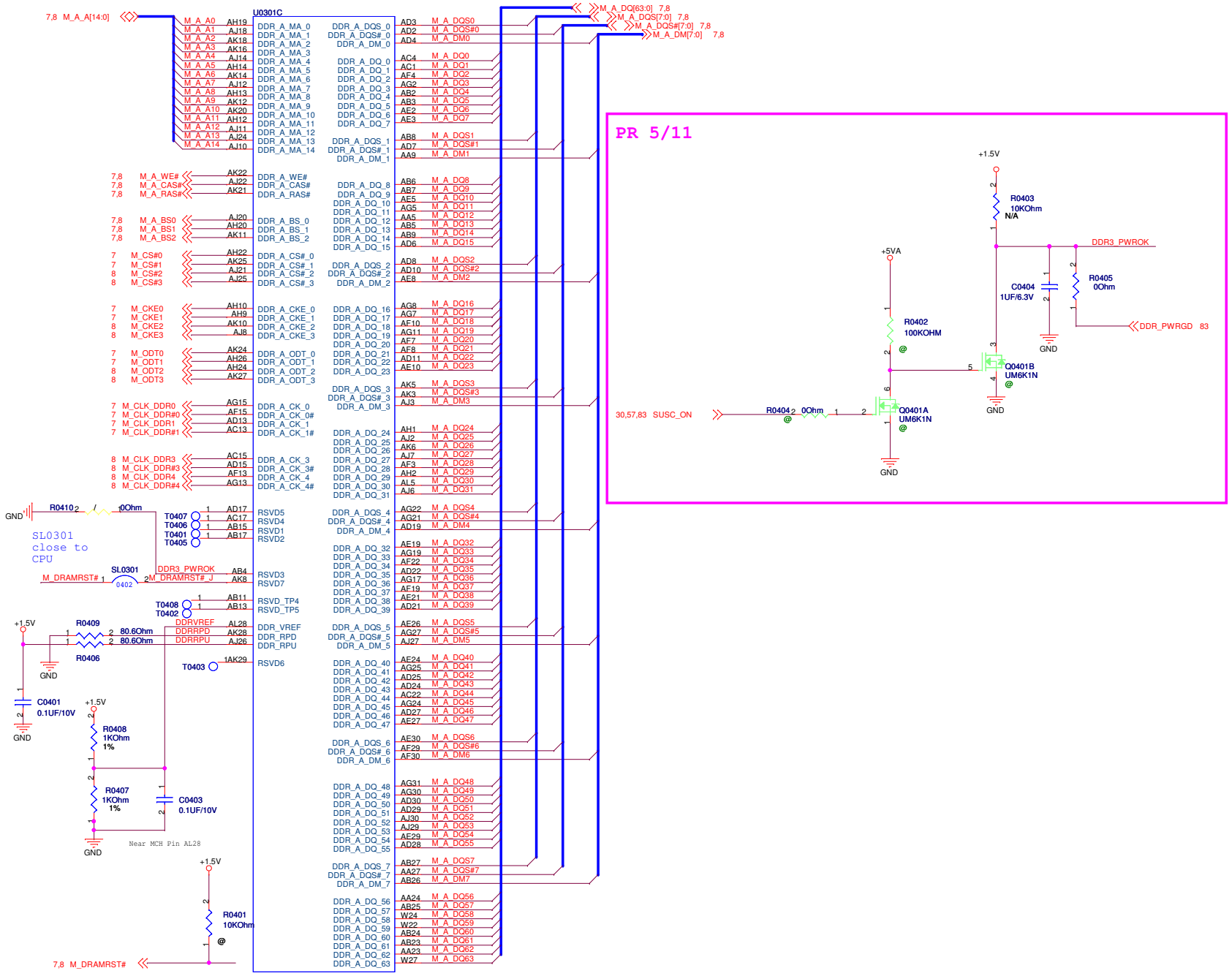
Size	Project Name	Rev
C	1215	1.0

Date: Monday, May 24, 2010 Sheet 2 of 97



<Variant Name>

ASUSTek Computer INC.	Title : PineView_1	
	Engineer: Aries/Jesse	
Size: B	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 3 of 97	



<Variant Name>

ASUSTek Computer INC.

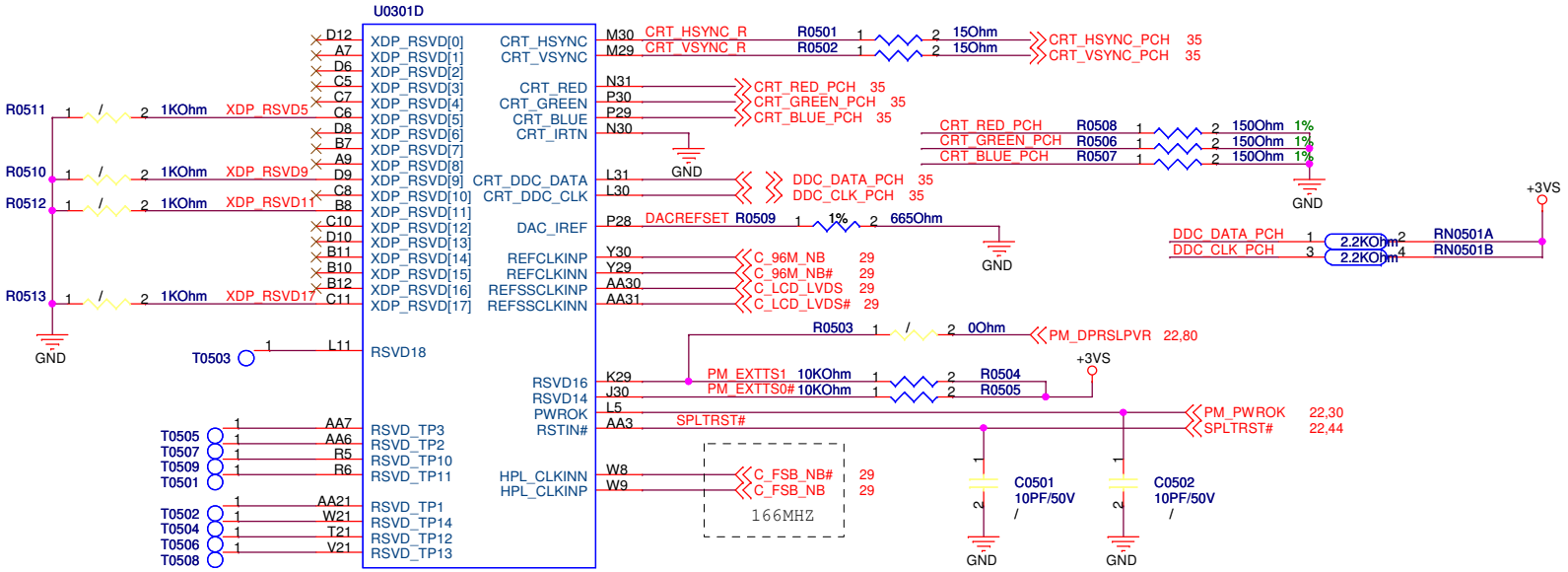
Title : PineView_2

Engineer: Aries/Jesse

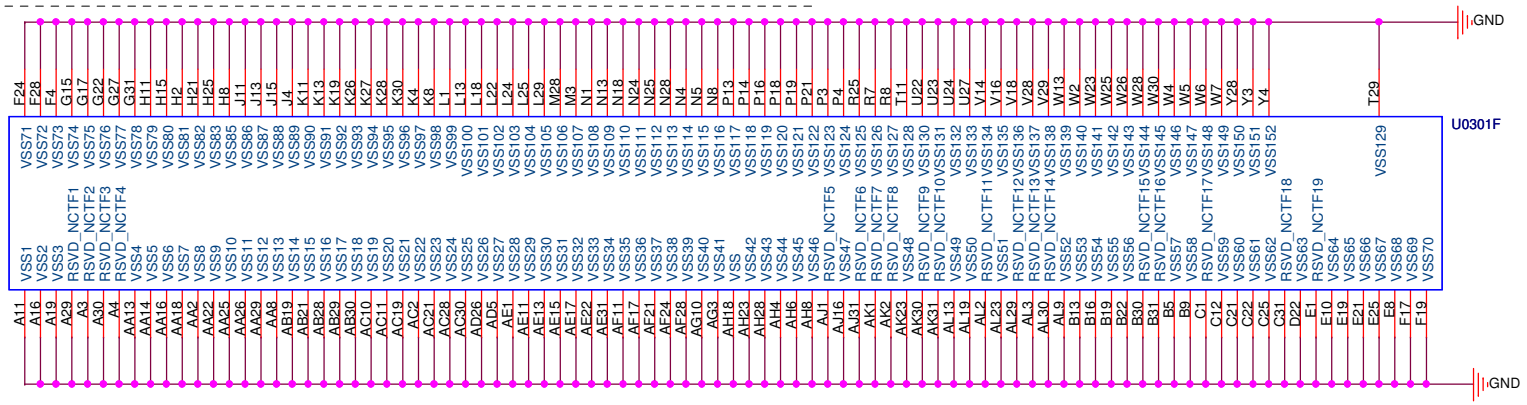
Size	Project Name	Rev
Custom	1215	1.0

Date: Monday, May 24, 2010 Sheet 4 of 97

DDC CLK&DATA need 2.2K Pull up to +3VS(Or may we can use 4.7K);connector side has pull-up resistor.



Intel confirm only RSVD9 need stuff 1K resistor.
D510 DMI x4 Strap PD:DMI X2 ; Umount:DMI X4



<Variant Name>

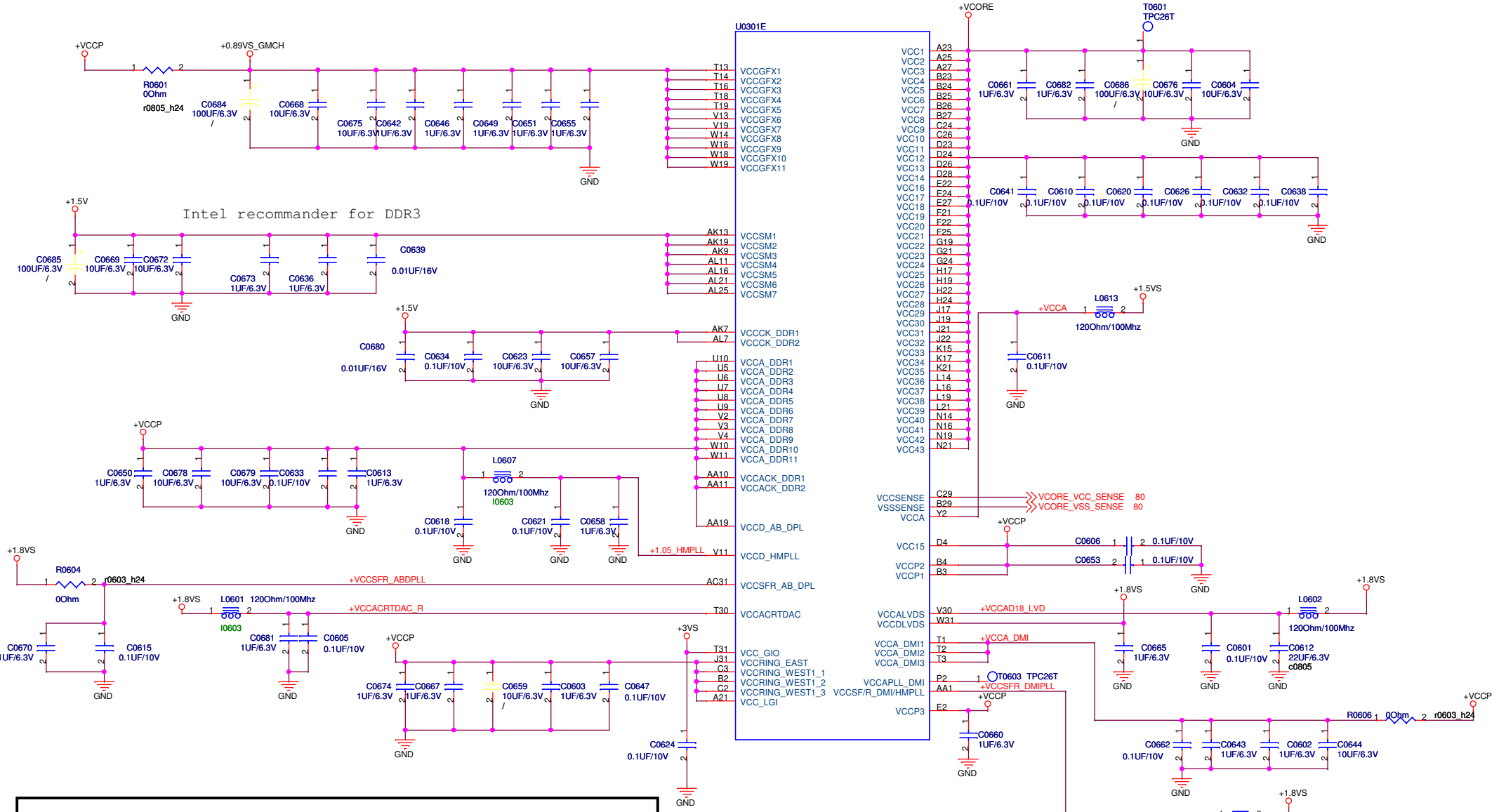
ASUSTek Computer INC.

Title : PineView_3

Engineer: Aries/Jesse

Size	Project Name	Rev
Custom	1215	1.0

Date: Monday, May 24, 2010 Sheet 5 of 97


U0301E
+VCCP
+0.89VS_GMCH
R0601
0Ohm
r0805_h24
C0684
100UF/6.3V
C0668
10UF/6.3V
C0675
10UF/6.3V
C0642
1UF/6.3V
C0646
1UF/6.3V
C0649
1UF/6.3V
C0651
1UF/6.3V
C0655
1UF/6.3V
GND
T13 VCCGFX1
T14 VCCGFX2
T16 VCCGFX3
T18 VCCGFX4
T19 VCCGFX5
V13 VCCGFX6
V19 VCCGFX7
W14 VCCGFX8
W16 VCCGFX9
W18 VCCGFX10
W19 VCCGFX11
+1.5V
Intel recommander for DDR3
C0685
100UF/6.3V
C0669
10UF/6.3V
C0672
10UF/6.3V
C0673
1UF/6.3V
C0636
1UF/6.3V
C0639
0.01UF/16V
AK13 VCCSM1
AK19 VCCSM2
AK9 VCCSM3
AL11 VCCSM4
AL16 VCCSM5
AL21 VCCSM6
AL25 VCCSM7
C0680
0.01UF/16V
C0634
0.1UF/10V
C0623
10UF/6.3V
C0657
10UF/6.3V
AK7 VCCCK_DDR1
AL7 VCCCK_DDR2
C0650
1UF/6.3V
C0678
10UF/6.3V
C0679
10UF/6.3V
C0633
0.1UF/10V
C0613
1UF/6.3V
L0607
120Ohm/100Mhz
I0603
C0618
0.1UF/10V
C0621
0.1UF/10V
C0658
1UF/6.3V
U10 VCCA_DDR1
U5 VCCA_DDR2
U6 VCCA_DDR3
U7 VCCA_DDR4
U8 VCCA_DDR5
U9 VCCA_DDR6
V2 VCCA_DDR7
V3 VCCA_DDR8
V4 VCCA_DDR9
W10 VCCA_DDR10
W11 VCCA_DDR11
AA10 VCCACK_DDR1
AA11 VCCACK_DDR2
AA19 VCCD_AB_DPL
+1.05_HMPLL
V11 VCCD_HMPLL
+1.8VS
R0604
0Ohm
r0603_h24
+VCCSFR_ABDPLL
AC31 VCCSFR_AB_DPL
C0670
1UF/6.3V
C0615
0.1UF/10V
L0601 120Ohm/100Mhz
I0603
+VCCACRTDAC_R
T30 VCCACRTDAC
C0681
1UF/6.3V
C0605
0.1UF/10V
+3VS
C0674
1UF/6.3V
C0667
1UF/6.3V
C0659
10UF/6.3V
C0603
1UF/6.3V
C0647
0.1UF/10V
T31 VCC_GIO
J31 VCCRING_EAST
C3 VCCRING_WEST1_1
B2 VCCRING_WEST1_2
C2 VCCRING_WEST1_3
A21 VCC_LGI
C0624
0.1UF/10V
+VCORE
T0601
TPC26T
VCC1 A23
VCC2 A25
VCC3 A27
VCC4 B23
VCC5 B24
VCC6 B25
VCC7 B26
VCC8 B27
VCC9 C24
VCC10 C26
VCC11 D23
VCC12 D24
VCC13 D26
VCC14 D28
VCC16 F22
VCC17 F24
VCC18 E27
VCC19 F21
VCC20 F22
VCC21 F25
VCC22 G19
VCC23 G21
VCC24 G24
VCC25 H17
VCC26 H19
VCC27 H22
VCC28 H24
VCC29 J17
VCC30 J19
VCC31 J21
VCC32 J22
VCC33 K15
VCC34 K17
VCC35 K21
VCC36 L14
VCC37 L16
VCC38 L19
VCC39 L21
VCC40 N14
VCC41 N16
VCC42 N19
VCC43 N21
C0661
1UF/6.3V
C0682
1UF/6.3V
C0686
100UF/6.3V
C0676
10UF/6.3V
C0604
10UF/6.3V
C0641
0.1UF/10V
C0610
0.1UF/10V
C0620
0.1UF/10V
C0626
0.1UF/10V
C0632
0.1UF/10V
C0638
0.1UF/10V
+1.5VS
L0613
120Ohm/100Mhz
+VCCA
C0611
0.1UF/10V
VCCSENSE C29
VSSSENSE B29
VCCA Y2
VCORE_VCC_SENSE 80
VCORE_VSS_SENSE 80
VCC15 D4
VCCP2 B4
VCCP1 B3
C0606
0.1UF/10V
C0653
0.1UF/10V
VCCALVDS V30
VCCDLVDS W31
+VCCAD18_LVD
+1.8VS
L0602
120Ohm/100Mhz
C0665
1UF/6.3V
C0601
0.1UF/10V
C0612
22UF/6.3V
c0805
VCCA_DMI1 T1
VCCA_DMI2 T2
VCCA_DMI3 T3
+VCCA_DMI
VCCAPLL_DMI P2
VCCSF/R_DMI/HMPLL AA1
T0603 TPC26T
+VCCSFR_DMIPLL
VCCP3 E2
C0660
1UF/6.3V
R0606 0Ohm r0603_h24
C0662
0.1UF/10V
C0643
1UF/6.3V
C0602
1UF/6.3V
C0644
10UF/6.3V
C0677
1UF/6.3V
L0609
120Ohm/100Mhz
I0603
VCC = 3.5A
VCCA =0.08A
VCCGFX =1.38A
VCCALVDS , VCCDLVDS=0.06A
VCCA_DMI =0.48A
VCCSFR_DMIHMPLL =0.104A
VCCA_DDR and VCCACK_DDR =1.32A
VCCSM and VCCCK_DDR =2.27A
VCCRING_EAST , VCCRING_EAST_WEST , VCC_LGI , VCCD_AB_DPL , VCCD_HMPLL =0.33A
VCC_GIO =0.006A
VCCSFR_AB_DPL , VCCACRTDAC =0.154A
Current for PineView
1bios.ru
<Variant Name>
Title : PineView_3
ASUSTek Computer INC.
Engineer: Aries/Jesse
Size Custom
Project Name 1215
Rev 1.0
Date: Monday, May 24, 2010
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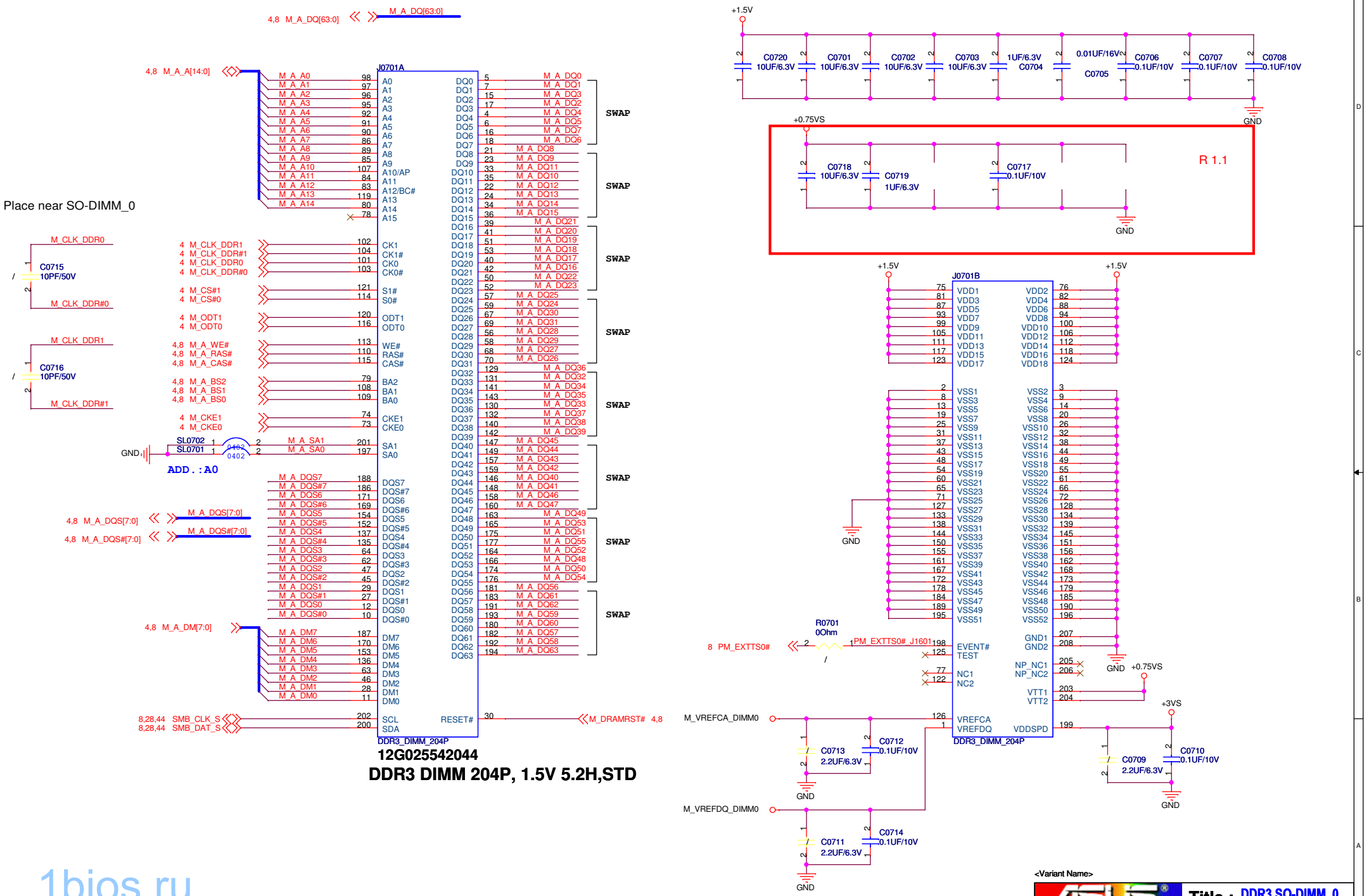
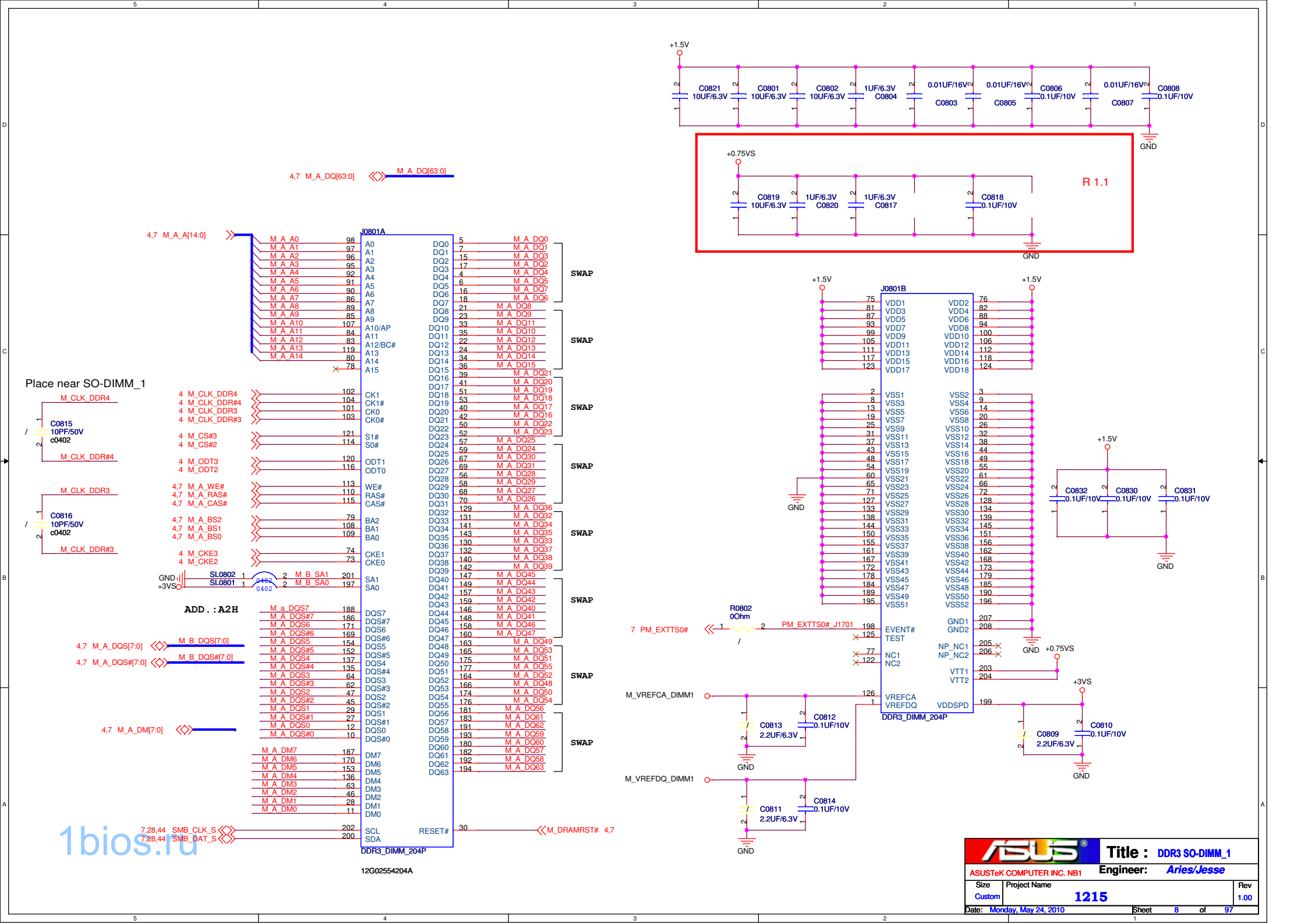


12G025542044

DDR3 DIMM 204P, 1.5V 5.2H,STD

<Variant Name>

ASUSTek Computer INC.	Title : DDR3 SO-DIMM_0	
	Engineer: Aries/Jesse	
Size: Custom	Project Name: 1215	Rev: 1.2G
Date: Monday, May 24, 2010	Sheet 7 of 97	


+1.5V
C0821 10UF/6.3V
C0801 10UF/6.3V
C0802 10UF/6.3V
1UF/6.3V C0804
0.01UF/16V C0803
0.01UF/16V C0805
C0806 0.1UF/10V
0.01UF/16V C0807
C0808 0.1UF/10V
GND
+0.75VS
C0819 10UF/6.3V
1UF/6.3V C0820
1UF/6.3V C0817
C0818 0.1UF/10V
R 1.1
GND
4,7 M_A_DQ[63:0]
M_A_DQ[63:0]
4,7 M_A_A[14:0]
J0801A
Place near SO-DIMM_1
M_CLK_DDR4
C0815 10PF/50V c0402
M_CLK_DDR#4
M_CLK_DDR3
C0816 10PF/50V c0402
M_CLK_DDR#3
4 M_CLK_DDR4
4 M_CLK_DDR#4
4 M_CLK_DDR3
4 M_CLK_DDR#3
4 M_CS#3
4 M_CS#2
4 M_ODT3
4 M_ODT2
4,7 M_A_WE#
4,7 M_A_RAS#
4,7 M_A_CAS#
4,7 M_A_BS2
4,7 M_A_BS1
4,7 M_A_BS0
4 M_CKE3
4 M_CKE2
SL0802
SL0801
M_B_SA1
M_B_SA0
GND
+3VS
ADD.:A2H
4,7 M_A_DQS[7:0]
4,7 M_A_DQS#[7:0]
M_B_DQS[7:0]
M_B_DQS#[7:0]
4,7 M_A_DM[7:0]
7,28,44 SMB_CLK_S
7,28,44 SMB_DAT_S
M_DRAMRST# 4,7
SWAP
DDR3_DIMM_204P
12G02554204A
1bios.ru
+1.5V
J0801B
GND
+0.75VS
+3VS
C0832 0.1UF/10V
C0830 0.1UF/10V
C0831 0.1UF/10V
R0802 0Ohm
7 PM_EXTTS0#
PM_EXTTS0#_J1701
M_VREFCA_DIMM1
M_VREFDQ_DIMM1
C0813 2.2UF/6.3V
C0812 0.1UF/10V
C0811 2.2UF/6.3V
C0814 0.1UF/10V
C0809 2.2UF/6.3V
C0810 0.1UF/10V
DDR3_DIMM_204P
ASUSTeK COMPUTER INC. NB1
Title : DDR3 SO-DIMM_1
Engineer: Aries/Jesse
Size Custom
Project Name 1215
Rev 1.00
Date: Monday, May 24, 2010
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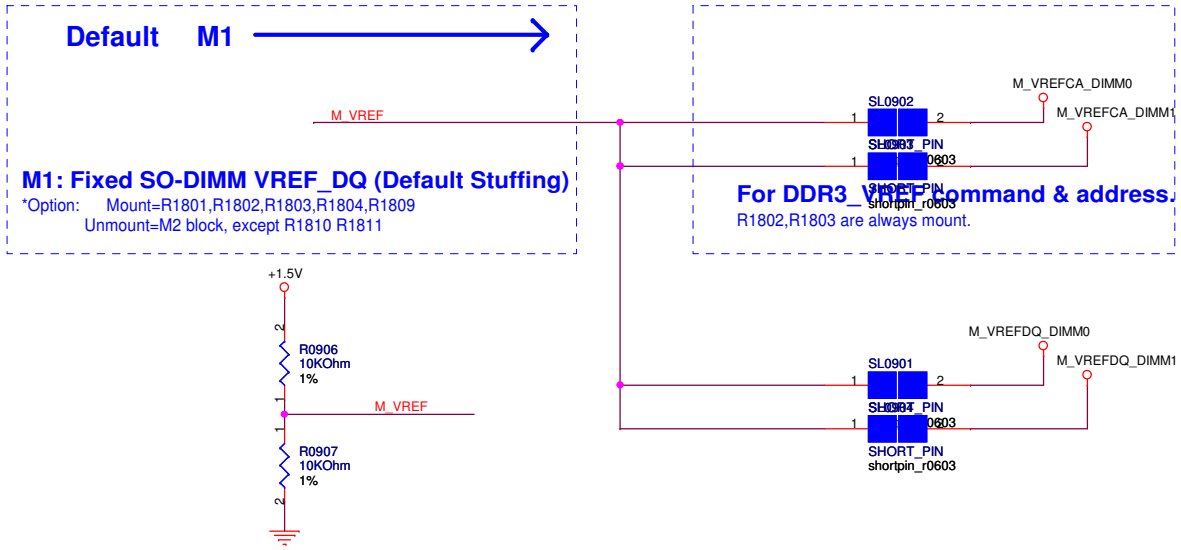


ASUSTeK COMPUTER INC. NB1	Title : DDR3 Vref	
	Engineer: Aries/Jesse	
Size: B	Project Name: 1215	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 9 of 97	

Main Board

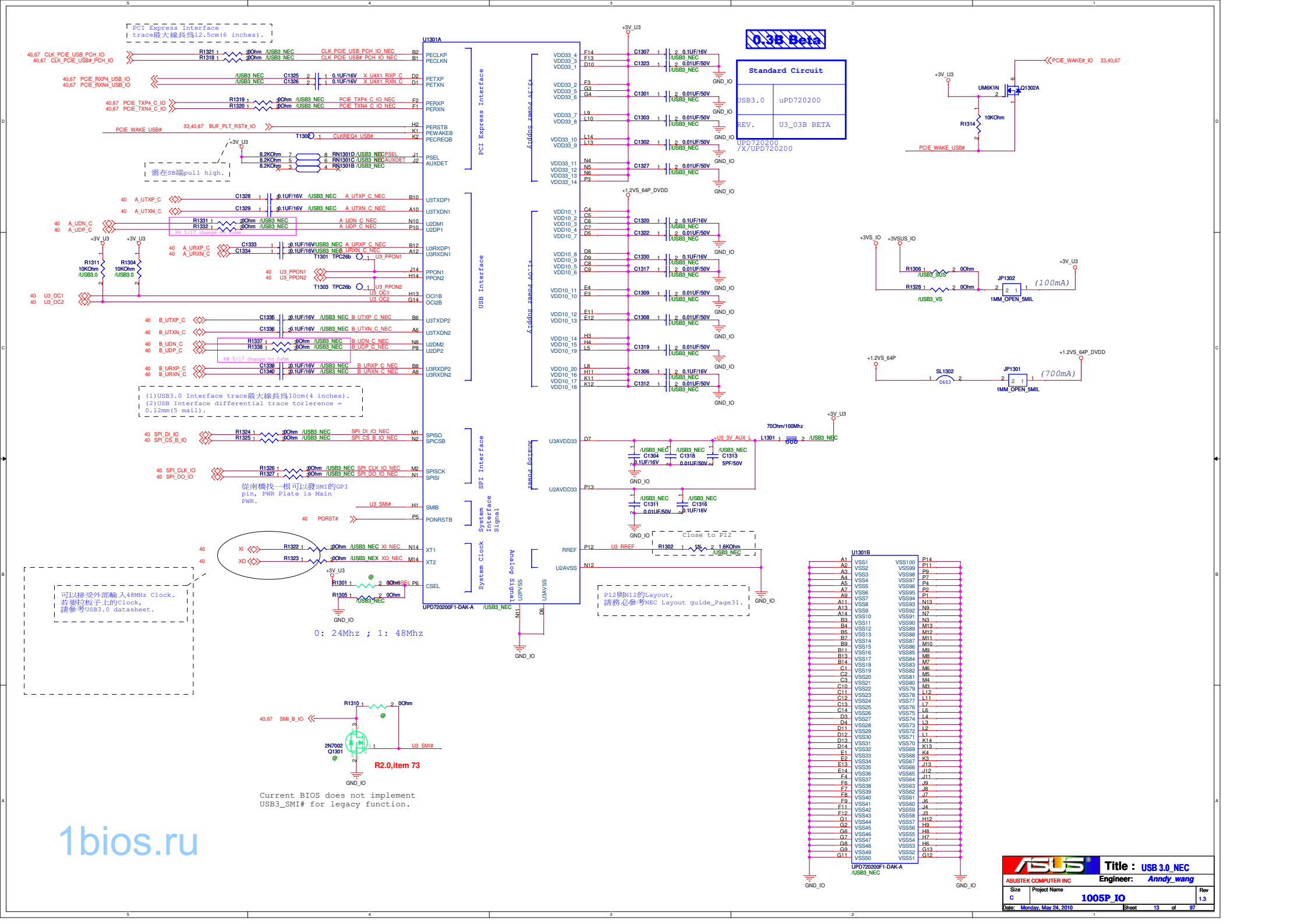
ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: ***	
Size: Custom	Project Name: 1215	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 10 of 97	

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: ***	
Size: Custom	Project Name: 1215	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 11 of 97	

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: ***	
Size: Custom	Project Name: 1215	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 12 of 97	


0.3B Beta
Standard Circuit
USB3.0 uPD720200
REV. U3_03B BETA
UPD720200 /X/UPD720200
U1301A
PCI Express Interface
USB Interface
SPI Interface
System Clock
System Interface Signal
Analog Signal
+3.3V power supply
+1.8V power supply
Analog power
U1301B
UPD720200F1-DAK-A
PCI Express Interface trace最大線長爲12.5cm(6 inches).
需在SB端pull high.
(1)USB3.0 Interface trace最大線長爲10cm(4 inches).
(2)USB Interface differential trace torlerence = 0.12mm(5 mail).
從南橋找一根可以發SMI的GPI pin, PWR Plate is Main PWR.
可以接受外部輸入48MHz Clock.
若要拉板子上的Clock,
請參考USB3.0 datasheet.
0: 24Mhz ; 1: 48Mhz
P12與N12的Layout,
請務必參考NEC Layout guide_Page31.
Close to PI2
R2.0,item 73
Current BIOS does not implement USB3_SMI# for legacy function.
1bios.ru
Title : USB 3.0_NEC
ASUSTEK COMPUTER INC
Engineer: Anndy_wang
Size C
Project Name 1005P_IO
Rev 1.3
Date: Monday, May 24, 2010
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ASUSTeK COMPUTER INC. NB6	Title :	Engineer: ***
Size: A	Project Name: 1215	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 14 of 97	

ASUSTeK COMPUTER INC. NB6	Title :	Engineer: ***
Size: A	Project Name: 1215	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 15 of 97	

<Variant Name>

Title : DDR2-SO-DIMM

ASUSTek Computer INC.

Engineer: ***

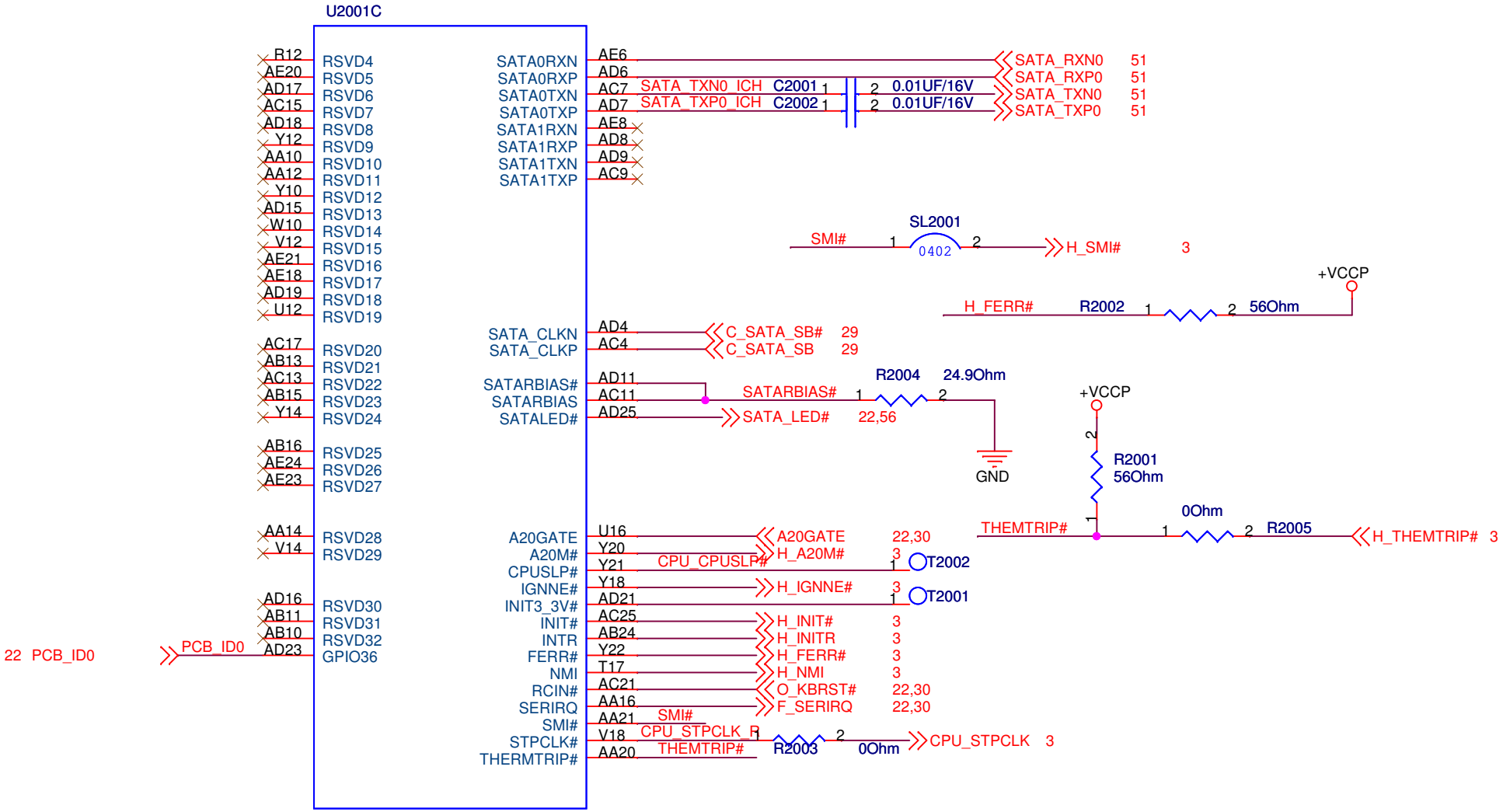
Size	Project Name	Rev
C	1215	1.2G

Date: Monday, May 24, 2010 Sheet 16 of 97

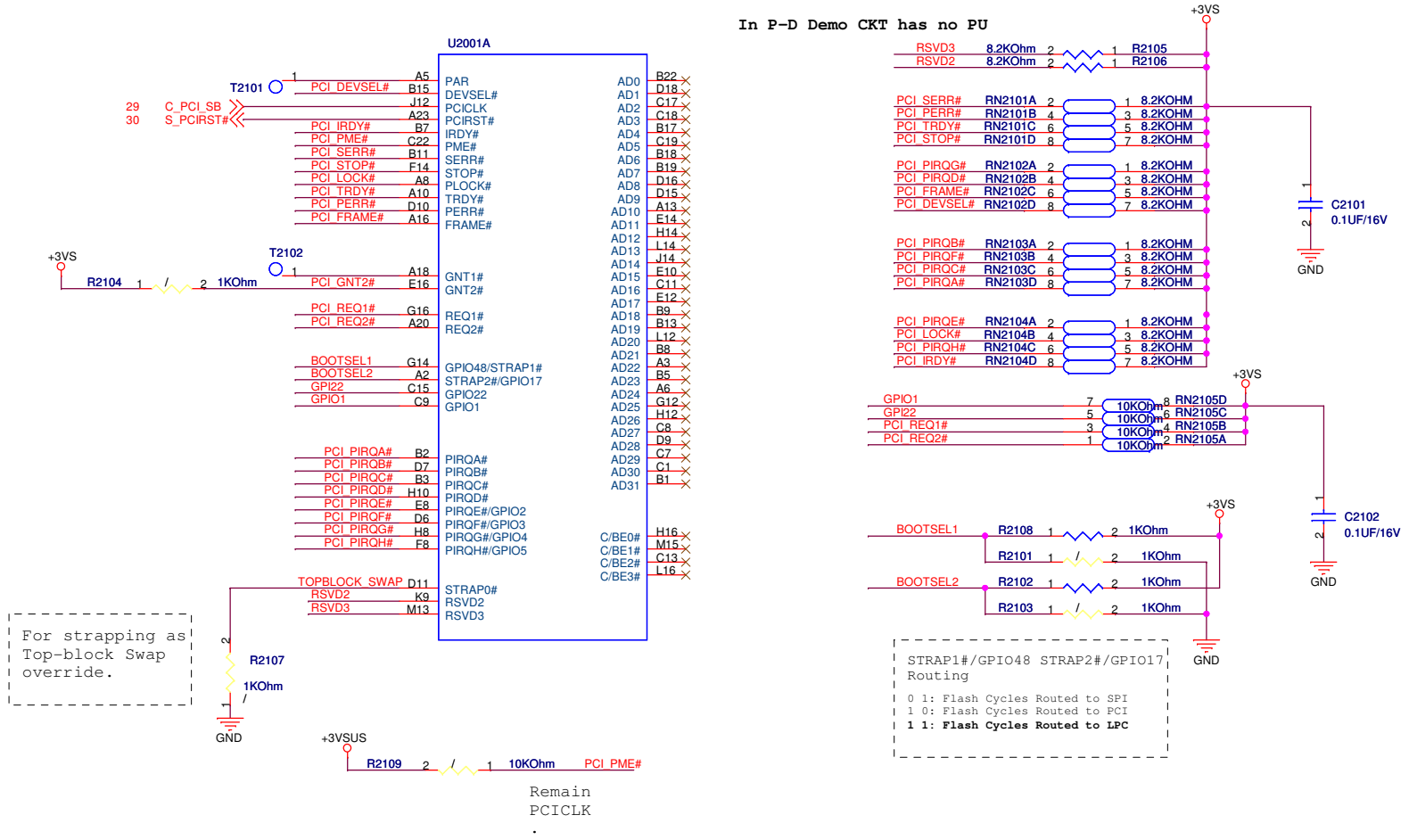
ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_1	
	Engineer: ***	
Size: C	Project Name: 1215	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 17 of 97	

ASUSTeK COMPUTER INC. NB6	Title DDR3 Vref	
	Engineer: ***	
Size: C	Project Name: 1215	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 18 of 97	

Title : VID Controller		
ASUSTeK COMPUTER INC. NB1	Engineer:	
Size: Custom	Project Name: 1215	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 19 of 97	



ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(1)SATA,IHDA,RTC,LPC	
	Engineer: Aries/Jesse	
Size: A	Project Name: 1215	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 20 of 97	



In P-D Demo CKT has no PU

<Variant Name>

ASUSTek Computer INC.	Title : PCH_IBEX(2)_PCIE,CLK,SMB,PEG	
	Engineer: Aries/Jesse	
Size: B	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 21 of 97	

CLK 14MHZ has a 22ohm resistor near clk Gen.

LDRQ0/1 LPC DMA/master request,ICH7M has internal PU, but we need TPT datasheet

SATA RX,TX all need AC couple and place near Connector side for signal quality.And Traces to them should match length. ICH7M need pull down RX, if no use.

Near Tigerpoint.

U2001B

USB INT PD 15K

If disable Port0,all PCIE port will be disable.

LAD[0:3] INT PU 20K

U2001D

SMI

Already 10K pull up to +3VS in clk gen section.

0 ohm for debugging later.

Place within 500 mils of ICH

DMI strap.

1=DMI interface is strapped to operate in DC coupled mode.
0=DMI interface is straped to operate in AC coupled mode.

Int PU 15K

Intel DEMO reserved pull-up and pull-down,but no explaintion , so will check with Intel

PCB_IO 0:dGPU
1:Optimus

RTC well input requires pull down to reduce leakage from coin cell battery in G3.
Cann't float in G3.

Reserved as intel demo sck.

Buffer for PLTRST# signal

RTC power.

J2201

WTOB_CON_2P
SMD
12G17100002C

For Rechargeable solution: Mount R2229

<Variant Name>

ASUSTek Computer INC.

Title : PCH_IBEX(3)_FDI,DMI,SYS PWR

Engineer: Aries/Jesse

Size: Custom | Project Name: 1215 | Rev: 1.0

Date: Monday, May 24, 2010 | Sheet 22 of 97

ASUSTeK COMPUTER INC. NB6

Title: HDMI(4) DP,LVDS,CRT

Engineer: ***

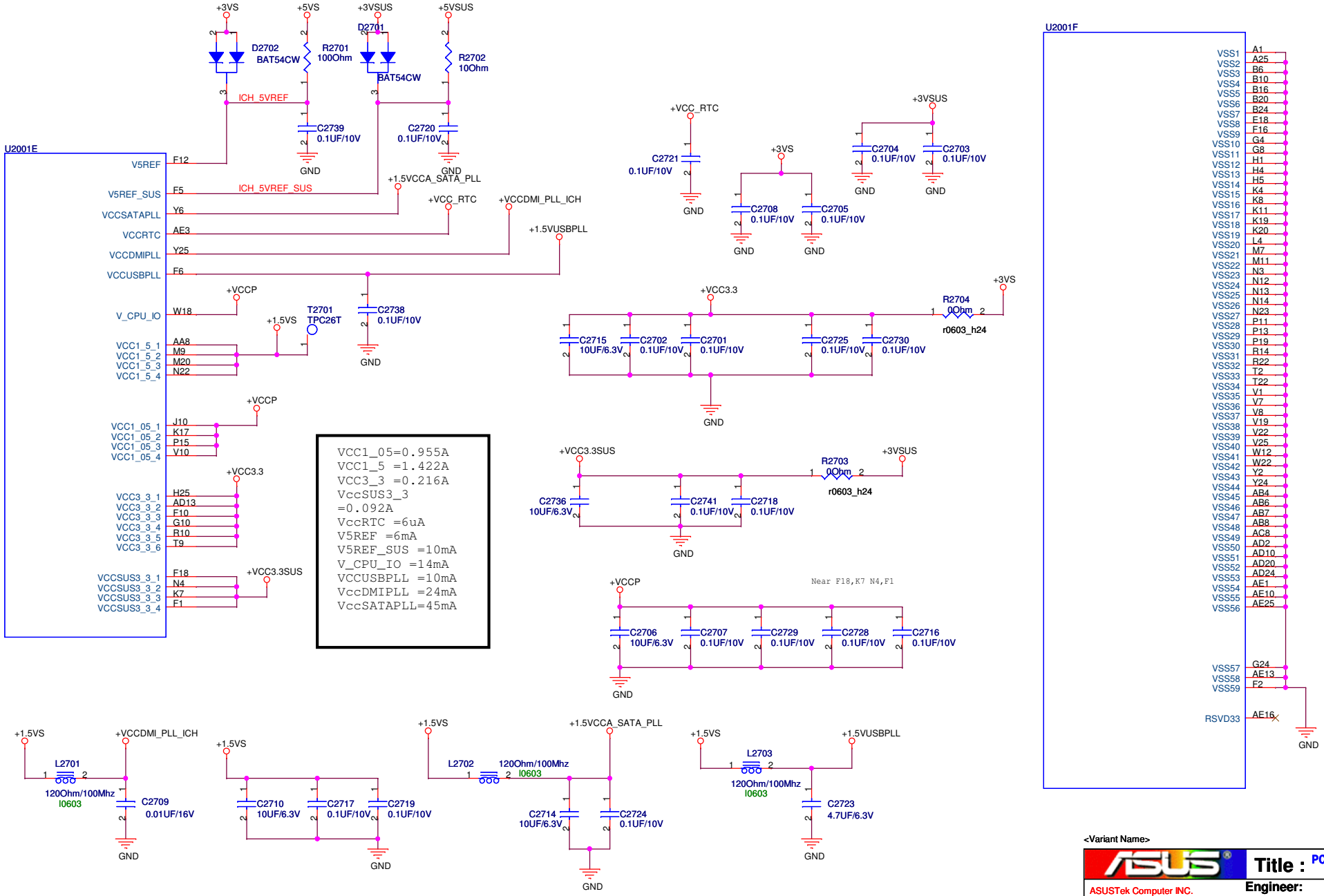
Size	Project Name	Rev
C	1215	1.00

Date: Monday, May 24, 2010 Sheet 23 of 97

ASUSTeK COMPUTER INC. NB6	Title : PCH IBEXS CH,NVRAM,USB	
	Engineer: ***	
Size: C	Project Name: 1215	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 24 of 97	

ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(6)CPU,GPIO,MISC,GND	
	Engineer: CH_Lin	
Size: C	Project Name: UL30AD	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 25 of 97	

ASUSTeK COMPUTER INC. NB6	Title: CR_IREX(7)_POWER,GND	
	Engineer: ***	
Size: C	Project Name: 1215	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 26 of 97	



<Variant Name>

Title : PCH_IBEX(8)_POWER,GND

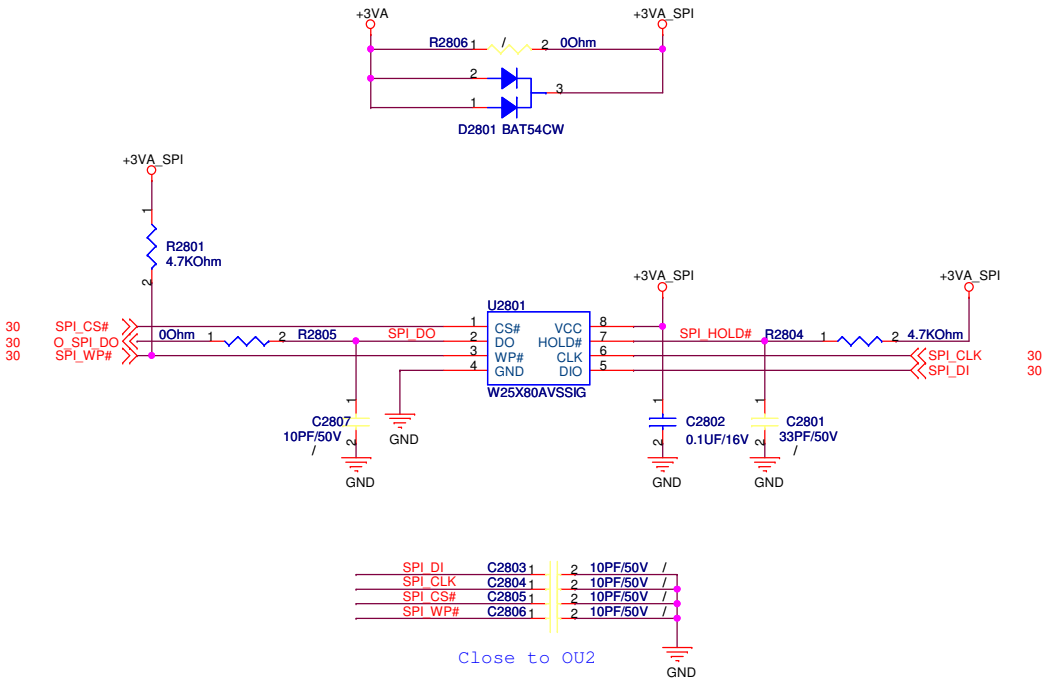
ASUSTek Computer INC. Engineer: Aries/Jesse

Size	Project Name	Rev
B	1215	1.0

Date: Monday, May 24, 2010 Sheet 27 of 97

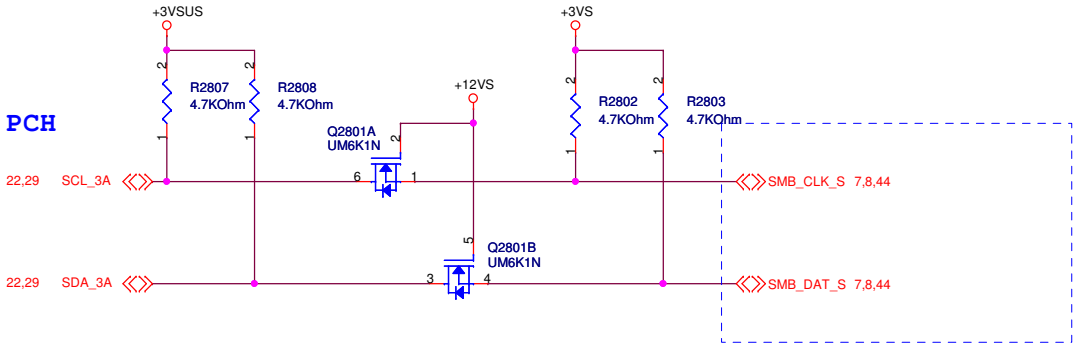
PCH SPI ROM

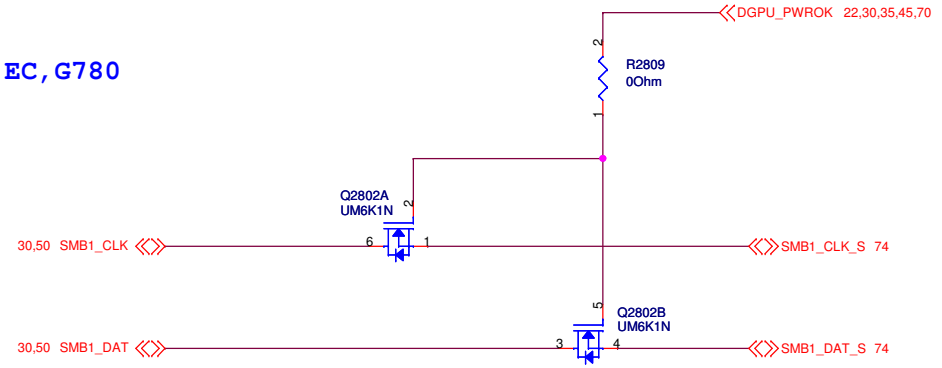
No SPI FLASH TOOL CON



SMBUS Link device:

SPD, CLKGEN, CPU XDP,PCH XDP,
VID CONTROLLER, DDRVref



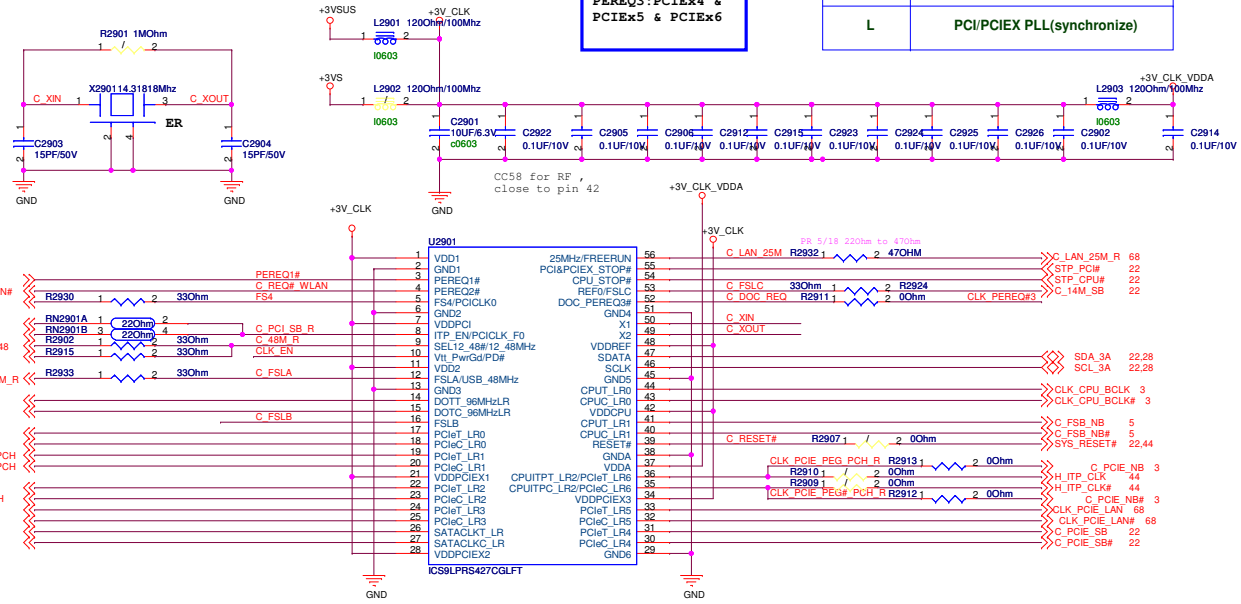


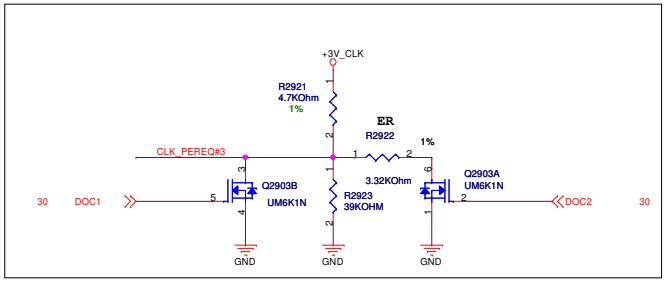
ASUSTeK COMPUTER INC. NB6	Title :PCH_SPI ROM,OTH	
	Engineer: Aries/Jesse	
Size: Custom	Project Name: 1215	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 28 of 97	

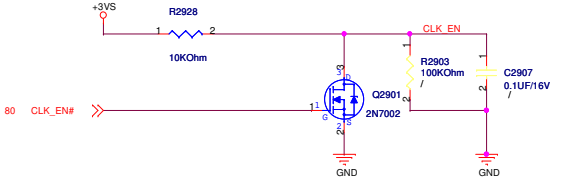
1:Disable
0:Enable

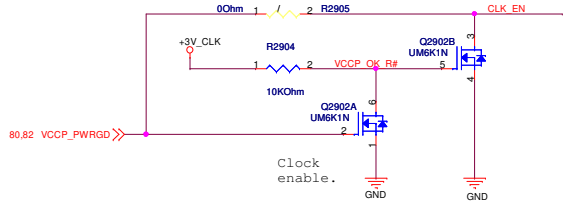
PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

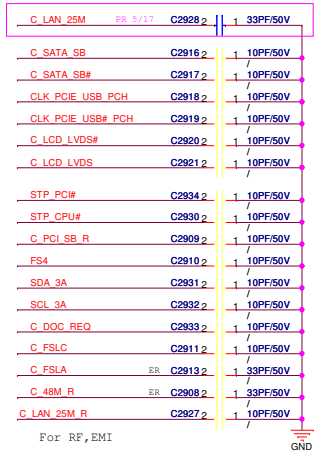
FS4	Function
H	FIXED PLL (Asynchronous)
L	PCI/PCIEX PLL(synchronize)

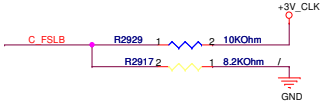


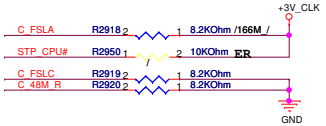


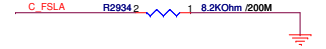


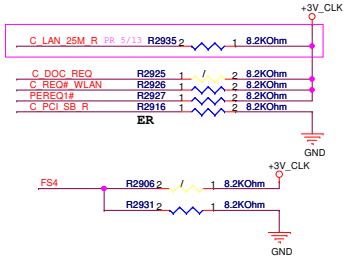












O_DOC1	O_DOC2	Voltage	Status
L	L	2.4-3.3V	Super
L	H	0.5-2.36V	Normal
H	*	0-0.35V	Power saving

FSLC	FSLB	FSLA	CPU(MHZ)
0	1	1	166
0	0	1	133
0	1	0	200

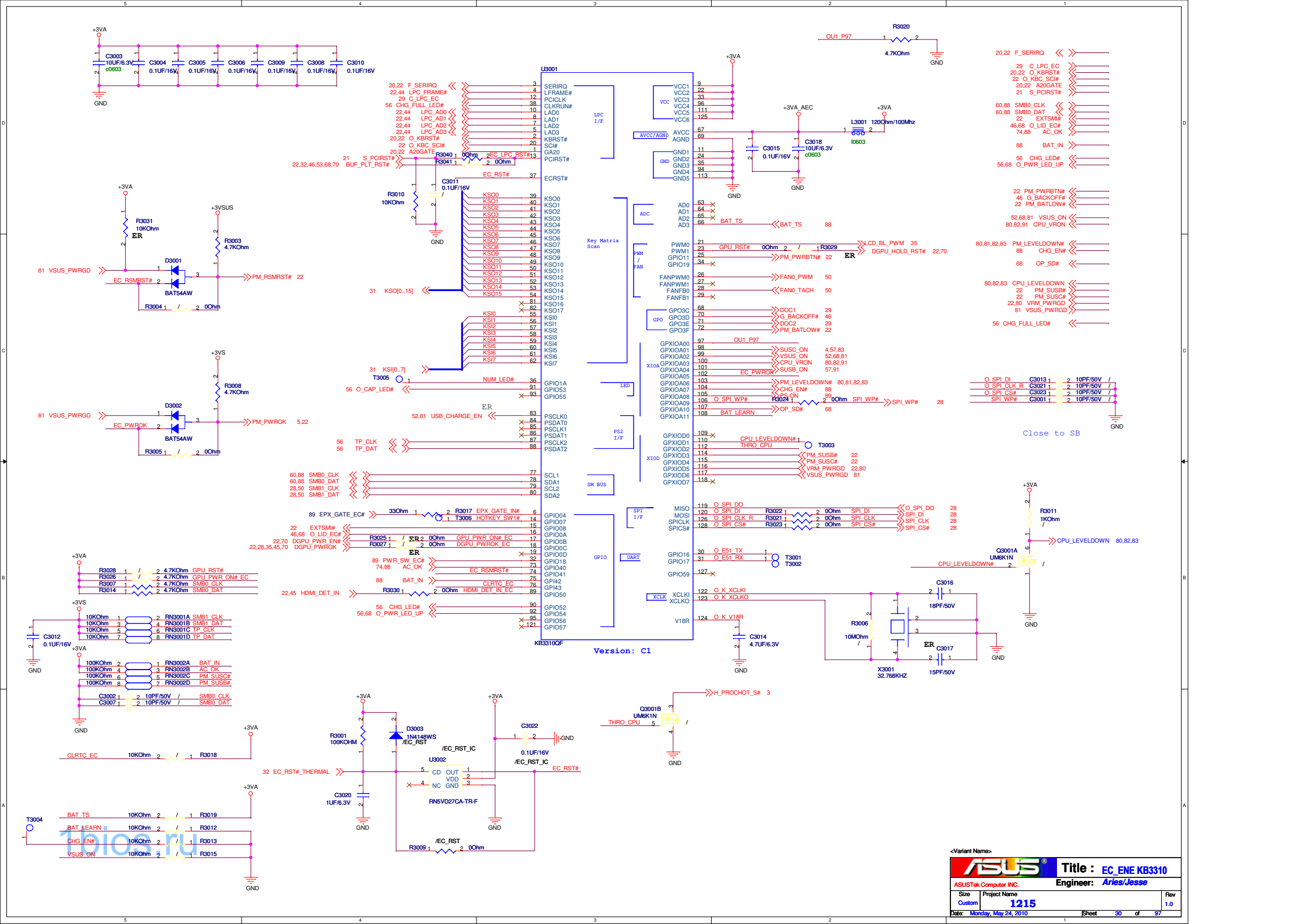
ASUSTeK COMPUTER INC. NB4

Title : CLK_ICS9LPRS427CGLFT

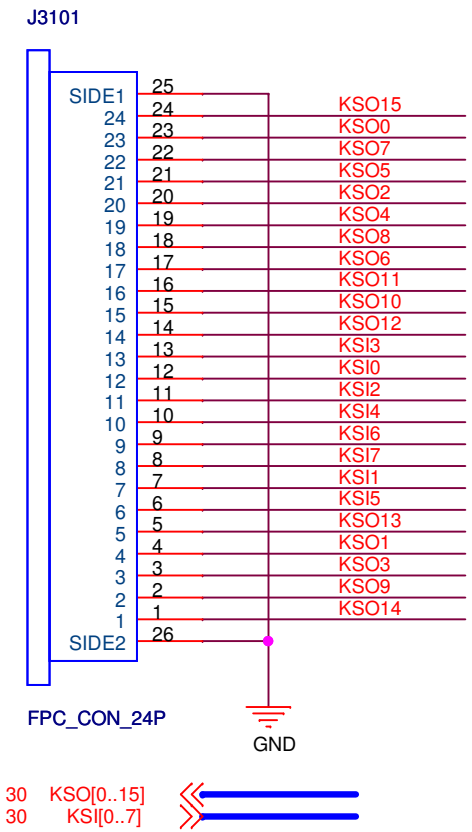
Engineer: Aries/Jesse

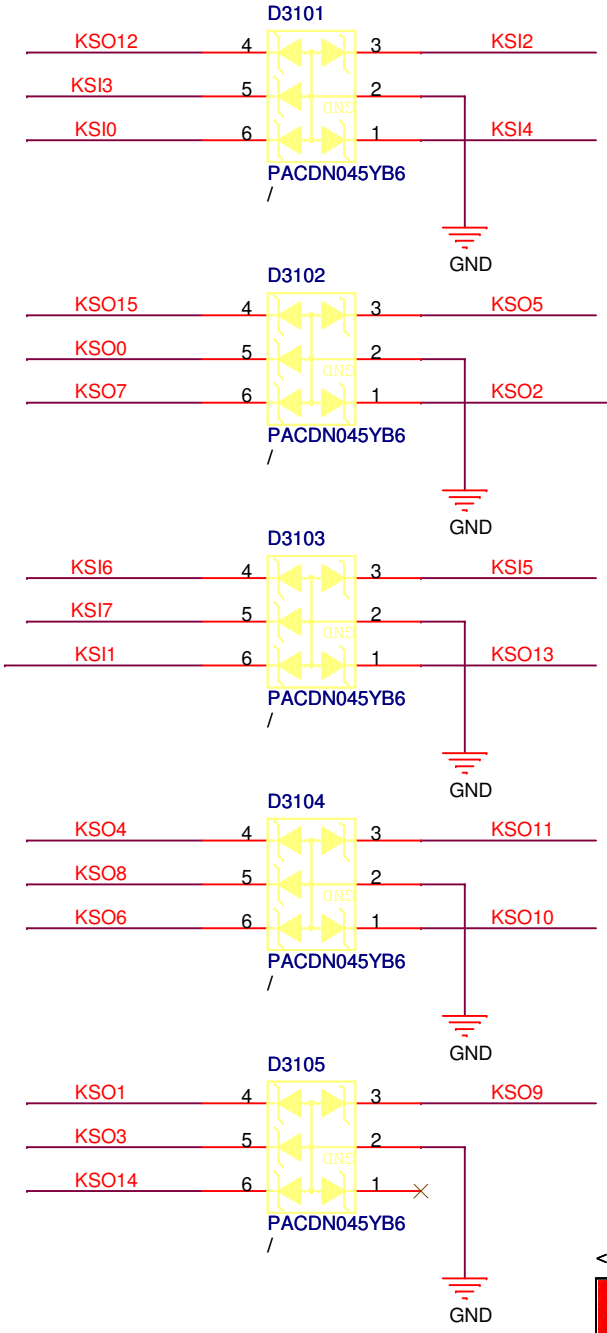
Size	Project Name	Rev
Custom	1215	1.00

Date: Monday, May 24, 2010 Sheet 29 of 97


U3001
KB3310QF
Version: C1
Close to SB
Key Matrix Scan
LPC I/F
PS2 I/F
SM BUS
SPI I/F
UART
ADC
FAN
GPIO
LED
XIOA
XIOD
XCLK
VCC
AVCC/AGND
GND
SERIRQ
LFRAME#
PCICLK
CLKRUN#
LAD0
LAD1
LAD2
LAD3
KBRST#
SCI#
GA20
PCIRST#
ECRST#
KSO0
KSO1
KSO2
KSO3
KSO4
KSO5
KSO6
KSO7
KSO8
KSO9
KSO10
KSO11
KSO12
KSO13
KSO14
KSO15
KSO16
KSO17
KSI0
KSI1
KSI2
KSI3
KSI4
KSI5
KSI6
KSI7
GPIO1A
GPIO53
GPIO55
PSCLK0
PSDAT0
PSCLK1
PSDAT1
PSCLK2
PSDAT2
SCL1
SDA1
SCL2
SDA2
GPIO04
GPIO07
GPIO08
GPIO0A
GPIO0B
GPIO0C
GPIO0D
GPIO18
GPIO40
GPIO41
GPI42
GPI43
GPIO50
GPIO52
GPIO54
GPIO56
GPIO57
AD0
AD1
AD2
AD3
BAT_TS
PWM0
PWM1
GPIO11
GPIO19
FANPWM0
FANPWM1
FANFB0
FANFB1
GPO3C
GPO3D
GPO3E
GPO3F
GPXIOA00
GPXIOA01
GPXIOA02
GPXIOA03
GPXIOA04
GPXIOA05
GPXIOA06
GPXIOA07
GPXIOA08
GPXIOA09
GPXIOA10
GPXIOA11
GPXIOD0
GPXIOD1
GPXIOD2
GPXIOD3
GPXIOD4
GPXIOD5
GPXIOD6
GPXIOD7
MISO
MOSI
SPICLK
SPICS#
GPIO16
GPIO17
GPIO59
XCLKI
XCLKO
V18R
O_K_XCLKI
O_K_XCLKO
O_K_V18R
+3VA
+3VA_AEC
+3VSUS
+3VS
C3003 10UF/6.3V c0603
C3004 0.1UF/16V
C3005 0.1UF/16V
C3006 0.1UF/16V
C3009 0.1UF/16V
C3008 0.1UF/16V
C3010 0.1UF/16V
C3011 0.1UF/16V
C3012 0.1UF/16V
C3013 10PF/50V
C3014 4.7UF/6.3V
C3015 0.1UF/16V
C3016 18PF/50V
C3017 15PF/50V
C3018 10UF/6.3V c0603
C3020 1UF/6.3V
C3021 10PF/50V
C3022 0.1UF/16V
C3023 10PF/50V
C3001 10PF/50V
C3002 10PF/50V
C3007 10PF/50V
L3001 120Ohm/100Mhz l0603
R3020 4.7KOhm
R3029 0Ohm ER
R3024 0Ohm
R3022 0Ohm
R3021 0Ohm
R3023 0Ohm
R3017 EPX_GATE_IN#
T3006 HOTKEY_SW1#
R3025 0Ohm GPU_PWR_ON# EC
R3027 0Ohm DGPU_PWROK_EC
R3030 0Ohm HDMI_DET_IN_EC
R3040 0Ohm EC_LPC_RST#
R3041 0Ohm
R3010 10KOhm
R3031 10KOhm ER
R3003 4.7KOhm
R3004 0Ohm
R3008 4.7KOhm
R3005 0Ohm
R3028 4.7KOhm GPU_RST#
R3026 4.7KOhm GPU_PWR_ON# EC
R3007 4.7KOhm SMB0_CLK
R3014 4.7KOhm SMB0_DAT
R3011 1KOhm
R3006 10MOhm
R3001 100KOHM
R3009 0Ohm /EC_RST
R3018 10KOhm CLRTC_EC
R3019 10KOhm BAT_TS
R3012 10KOhm BAT_LEARN
R3013 10KOhm CHG_EN#
R3015 10KOhm VSUS_ON
RN3001A SMB1_CLK
RN3001B SMB1_DAT
RN3001C TP_CLK
RN3001D TP_DAT
RN3002A BAT_IN
RN3002B AC_OK
RN3002C PM_SUSC#
RN3002D PM_SUSB#
RN5VD27CA-TR-F
D3001 BAT54AW
D3002 BAT54AW
D3003 1N4148WS /EC_RST
Q3001A UM6K1N
Q3001B UM6K1N
X3001 32.768KHZ
T3001
T3002
T3003
T3004
T3005
Title : EC_ENE KB3310
ASUSTek Computer INC.
Engineer: Aries/Jesse
Project Name 1215
Size Custom
Rev 1.0
Date: Monday, May 24, 2010
Sheet 30 of 97
<Variant Name>
1bios.ru

For Keyboard Connector

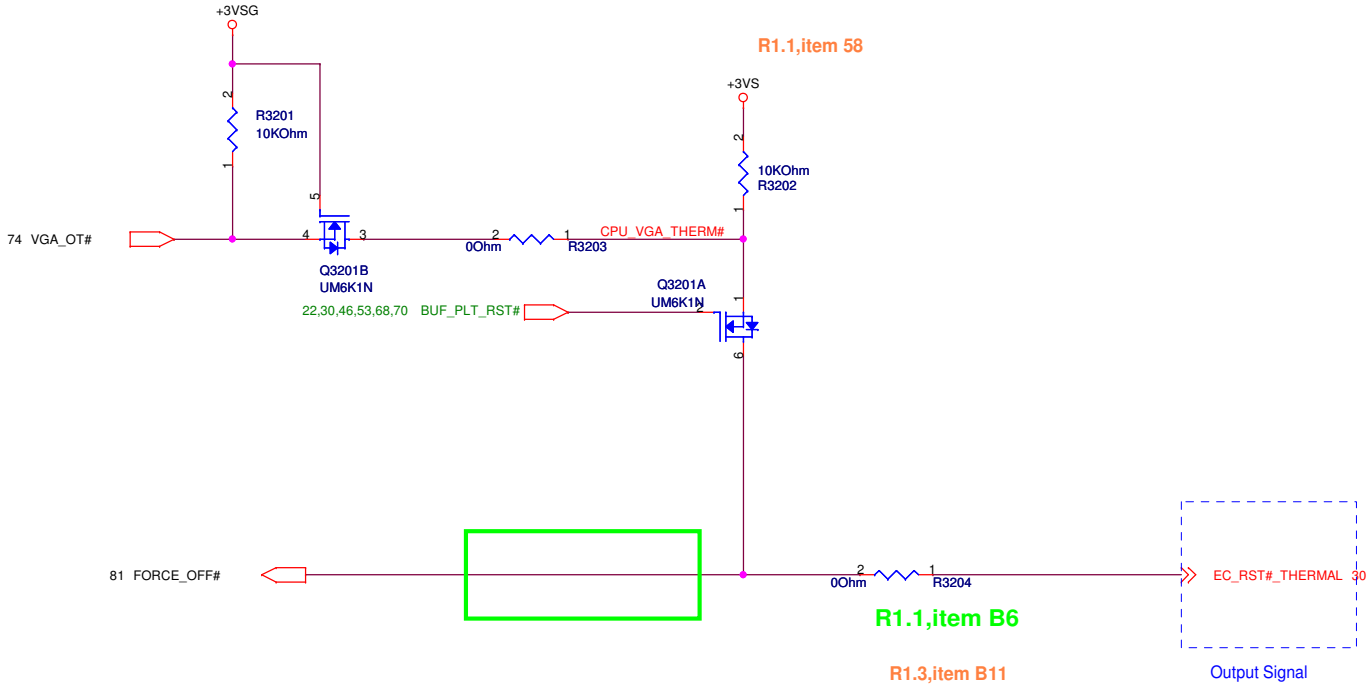




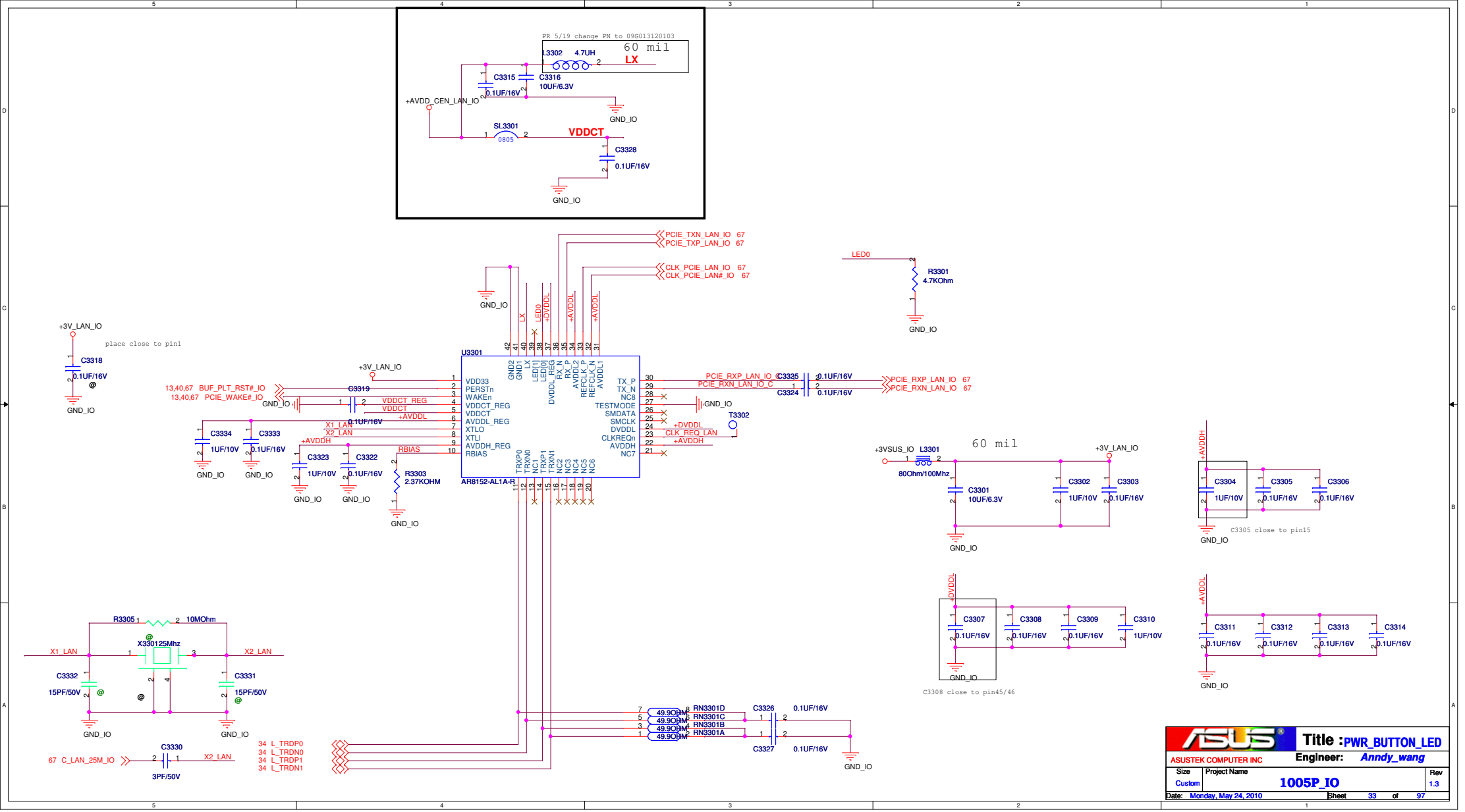
<Variant Name>

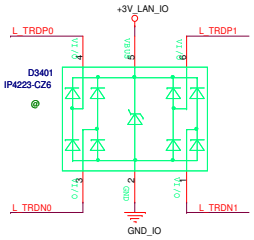
ASUSTeK COMPUTER INC	Title : KB	
	Engineer: Aries/Jesse	
Size: A	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 31 of 97	

Thermal Policy

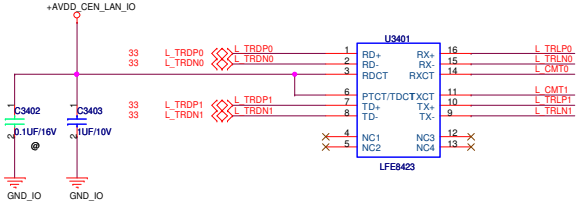


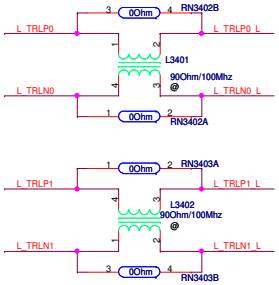
ASUSTeK COMPUTER INC. NB4	Title : RST_Reset Circuit	
	Engineer: Aries/Jesse	
Size: B	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 32 of 97	

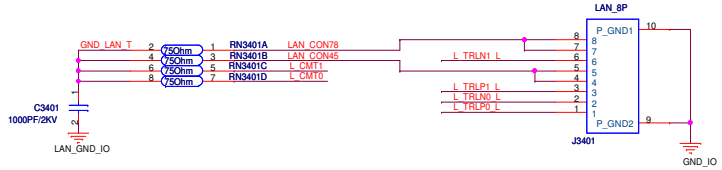

PR 5/19 change PN to 09G013120103
60 mil
L3302 4.7UH
LX
C3315 0.1UF/16V
C3316 10UF/6.3V
+AVDD_CEN_LAN_IO
GND_IO
SL3301 0805
VDDCT
C3328 0.1UF/16V
PCIE_TXN_LAN_IO 67
PCIE_TXP_LAN_IO 67
CLK_PCIE_LAN_IO 67
CLK_PCIE_LAN#_IO 67
LED0
R3301 4.7KOhm
+3V_LAN_IO
place close to pin1
C3318 0.1UF/16V
U3301
AR8152-AL1A-R
13,40,67 BUF_PLT_RST#_IO
13,40,67 PCIE_WAKE#_IO
C3319
VDDCT_REG
VDDCT
+AVDDL
X1_LAN
X2_LAN
+AVDDH
RBIAS
R3303 2.37KOHM
C3334 1UF/10V
C3333 0.1UF/16V
C3323 1UF/10V
C3322 0.1UF/16V
PCIE_RXP_LAN_IO_C
PCIE_RXN_LAN_IO_C
C3325 0.1UF/16V
C3324 0.1UF/16V
PCIE_RXP_LAN_IO 67
PCIE_RXN_LAN_IO 67
T3302
+DVDDL
CLK_REQ_LAN
+3VSUS_IO
L3301
80Ohm/100Mhz
60 mil
C3301 10UF/6.3V
C3302 1UF/10V
C3303 0.1UF/16V
C3304 1UF/10V
C3305 0.1UF/16V
C3306 0.1UF/16V
C3305 close to pin15
C3307 0.1UF/16V
C3308 0.1UF/16V
C3309 0.1UF/16V
C3310 1UF/10V
C3308 close to pin45/46
C3311 0.1UF/16V
C3312 0.1UF/16V
C3313 0.1UF/16V
C3314 0.1UF/16V
R3305 10MOhm
X3301 25Mhz
C3332 15PF/50V
C3331 15PF/50V
C3330 3PF/50V
67 C_LAN_25M_IO
34 L_TRDP0
34 L_TRDN0
34 L_TRDP1
34 L_TRDN1
RN3301D 49.9OHM
RN3301C 49.9OHM
RN3301B 49.9OHM
RN3301A 49.9OHM
C3326 0.1UF/16V
C3327 0.1UF/16V
Title :PWR_BUTTON_LED
ASUSTEK COMPUTER INC
Engineer: Anndy_wang
Size Custom
Project Name 1005P_IO
Rev 1.3
Date: Monday, May 24, 2010
Sheet 33 of 97

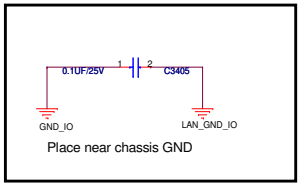


GND_LAN_T 上禁止加任何零件



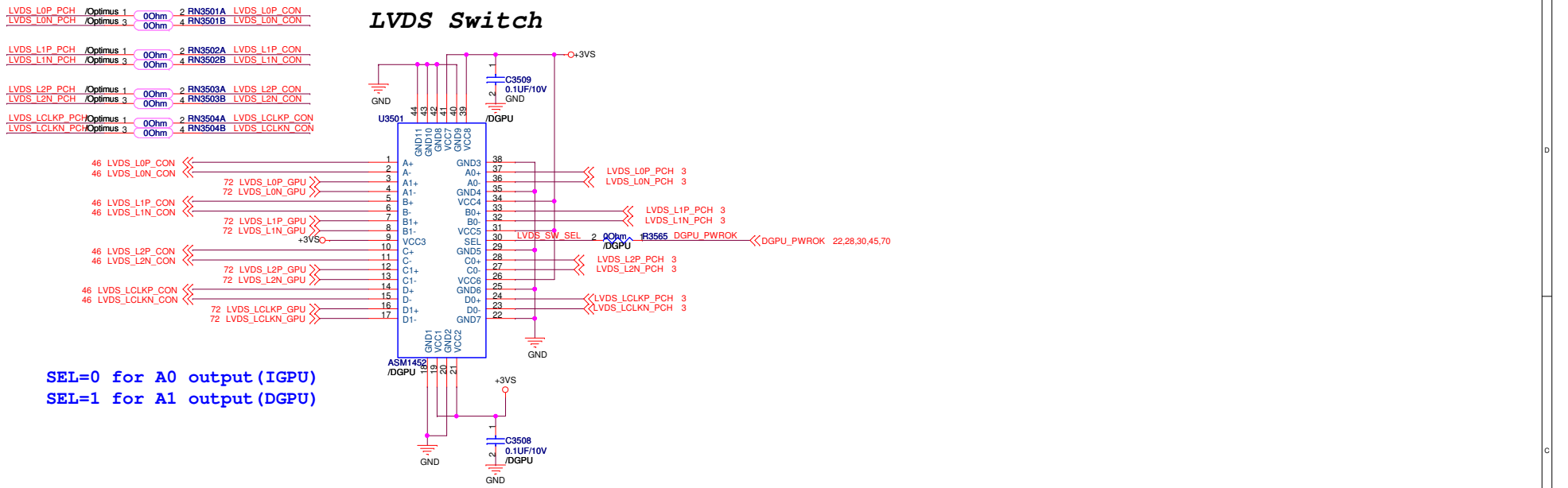






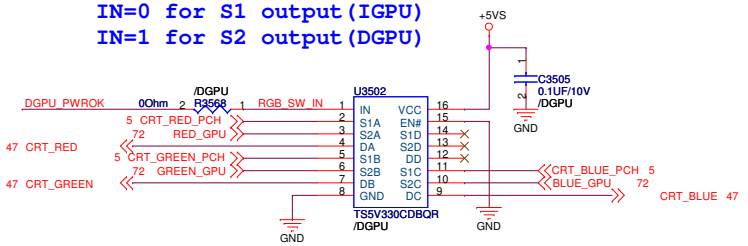
ASUSTEK COMPUTER INC	Title : PWR_BUTTON_LED	
	Engineer: Anndy_wang	
Size: C	Project Name: 1005P_IO	Rev: 1.3
Date: Monday, May 24, 2010	Sheet 34 of 97	

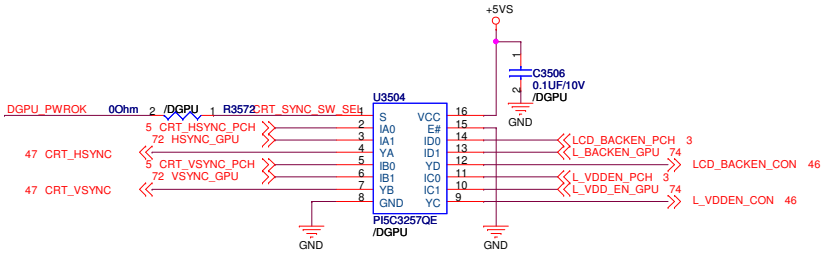
LVDS Switch

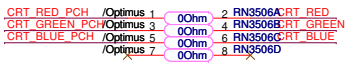


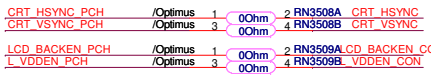
SEL=0 for A0 output(IGPU)
SEL=1 for A1 output(DGPU)

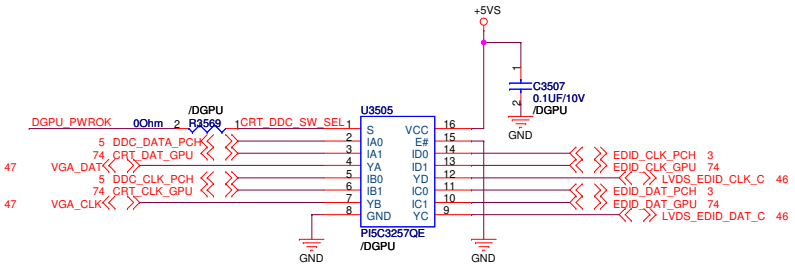
IN=0 for S1 output(IGPU)
IN=1 for S2 output(DGPU)

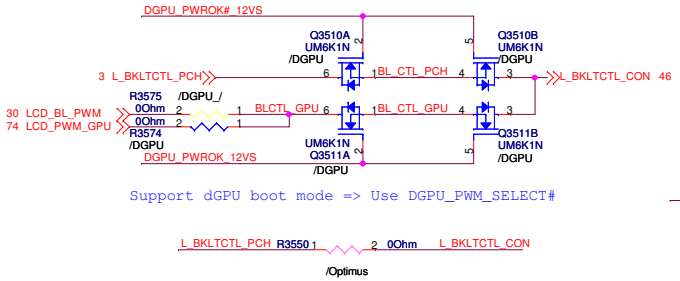


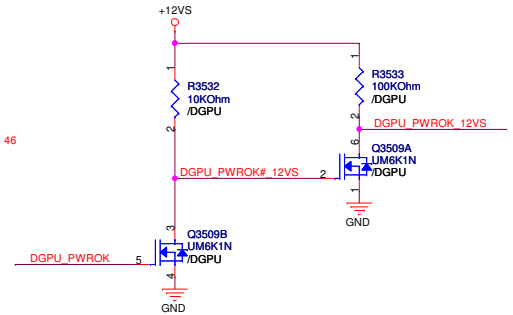


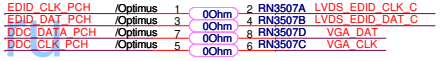












ASUSTeK COMPUTER INC. NB1

Title : Display Switch

Engineer: Aries/Jesse

Size	Project Name	Rev
Custom	1215	1.01

Date: Monday, May 24, 2010 Sheet 35 of 97

R1.7 ALC269-VB2 Issue
PD# is internal pull-up to 5VS_AUDIO & VIH=3.3V
Add R3602 &R3613 of PD# to make sure the PD# is higher than 3.3V when power up speaker amplifier

269VA USE 0 ohm/0603

37 DLY_OP_SD#
DLY_OP_SD# : "L" ==> PD# = 0.37V*H* ==> PD# = 3.55V
Q3601 PMBS3904 /269_VA/269_VB5

DVDD_IO
C3612 0.1UF/16V
C3611 10UF/10V
+5VS_AMP_IO
C3619 10UF/10V
C3620 1UF/10V
C3621 0.1UF/16V
L3601 80Ohm/100Mhz
+5VS_IO
GND_IO
5/26

6/29 DesignIP R1.3

D3601 AZ2015-01H.R7F
U3601 UP7714BMT5-00
Vref = 0.8V
R3609 0Ohm /269_VB
C3622 100PF/50V /269_VA
R3605 49.9KOhm 1%
R3602 10KOhm 1%
R3622 0Ohm
C3606 1UF/16V c0603
C3607 1UF/16V c0603
GND_AUDIO_IO

UP7714BMT5-00 (P/N:06G029330020)
Vout=0.8*(1+(49.9K/10K)
=4.792V

JP3602 SGL_JUMP
+3VS_IO
+1.5VS_IO
DVDD_IO

EMI 07/03

C3625 0.1UF/16V
C3604 0.1UF/16V
C3605 10UF/10V

U3602A ALC269Q-VA6-GR
U3602B ALC269Q-VA6-GR

H_SPKR+ H_SPKR- H_SPKL- H_SPKL+
C3602 0.1UF/16V
C3603 0.1UF/16V
EAPD

269_VA : 02G611005006
269_VB : 02G611005010

67 AZ_DMIC_DATA_IO
67 AZ_DMIC_CLK_IO
R3615 20Ohm AZ_DMIC_DATA_IO_R
R3616 20Ohm AZ_DMIC_CLK_IO_R
DLY_OP_SD#_R
67 AZ_SDOUT_AUD_IO
67 AZ_BCLK_AUD_IO
67 AZ_SDIN0_AUD_IO
R3604 33Ohm AZ_SDIN0_AUD_IO_R
67 AZ_SYNC_AUD_IO
37,67 AZ_RST#_AUD_IO
T3605 PC_BEEP
TPC26T

Place R3606 near U3602
Digital
GND
GND_AUDIO

C3617 2.2UF/10V
CPVEE
MIC_VREFOUT_L
MIC2_VREFOUT
LDO_CAP
VREF_CODEC
AC_HP_R
AC_HP_L
T3601
C3618 2.2UF/10V
C3615 1UF/10V
C3619 10UF/10V
C3616 2.2UF/10V
C3608 10UF/10V
C3609 0.1UF/16V

EMI 07/03

For VIA VT1802P
C3627、C3628 Change to 2.2UF/10V (P/N：11G233322536360)

For VIA VT1802P
C3615 Change to 0.1uF (P/N ：11G233310432340)
C3608 may improve the audio performance

R1.5 Co-lay for 269_VB
MIC_VREFOUT_L R3606 0Ohm /269_VB MIC1_VREFOUT_L 37
R3611 0Ohm /269_VA GND_AUDIO_IO
LDO_CAP R3610 0Ohm /269_VA MIC1_VREFOUT_L
C3624 10UF/10V /269_VB GND_AUDIO_IO

37 MIC1_JD R3607 20KOhm
37 LINE2_JD R3603 39.2KOhm
MIC2_VREFOUT C3626 1UF/10V
R3608 0Ohm /269_VA
AZ_DMIC_DATA_IO R3617 0Ohm
AZ_DMIC_DATA_IO_RA C3627 1UF/10V c0603 INTMIC_L
C3628 1UF/10V c0603 INTMIC_R
R3601 20KOhm
C6717 100PF/50V
MONO_OUT
JDREF

For VIA VT1802P
R3601 Change to 5.1Kohm (P/N：10G212510114030)

RealTek recommend change C3615 from 2.2uF to 1uF
New project : Please use the 1uF for VREF_CODEC
On going project : Please keep 2.2uF for VREF_CODEC if speaker have not S3、S4 resume issue.

For EMI
EMI 05/26
R3618 0Ohm
R3619 0Ohm
R3620 0Ohm
R3621 0Ohm
C3630 100PF/50V
R3623 0Ohm

T3602
37 MIC_IN_AC_E
TPC26T
C3613 2.2UF/10V
C3614 2.2UF/10V
MIC_IN_AC_E_L
MIC_IN_AC_E_R

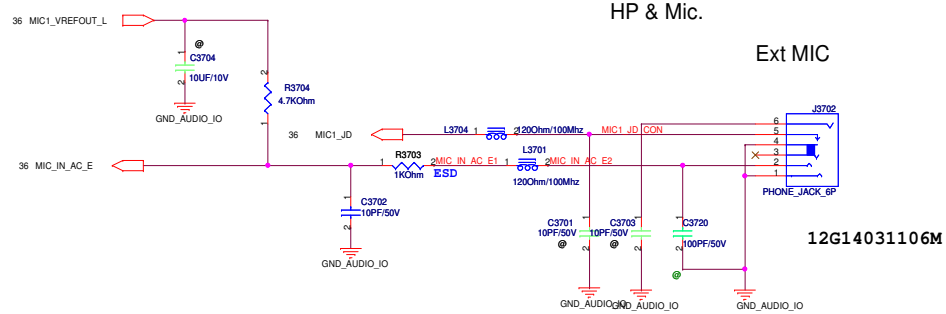
EMI 05/26
AZ_BCLK_AUD_IO C3623 10PF/50V @
06/19 remove PC beep
AZ_DMIC_CLK_IO_R C3629 0.1UF/16V @/EMI

For VIA VT1802P
Please reserve 11G232022004320 for AC2_BCLK_AUD at PCH (SB) side

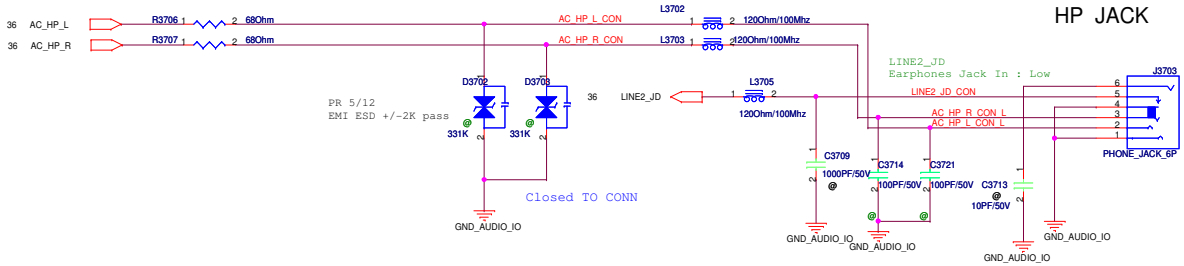
ASUSTEK COMPUTER INC	Title : ALC269-1	
	Engineer: Anndy_wang	
Size: C	Project Name: 1005P_IO	Rev: 1.3
Date: Monday, May 24, 2010	Sheet 36 of 97	

HP & Mic.

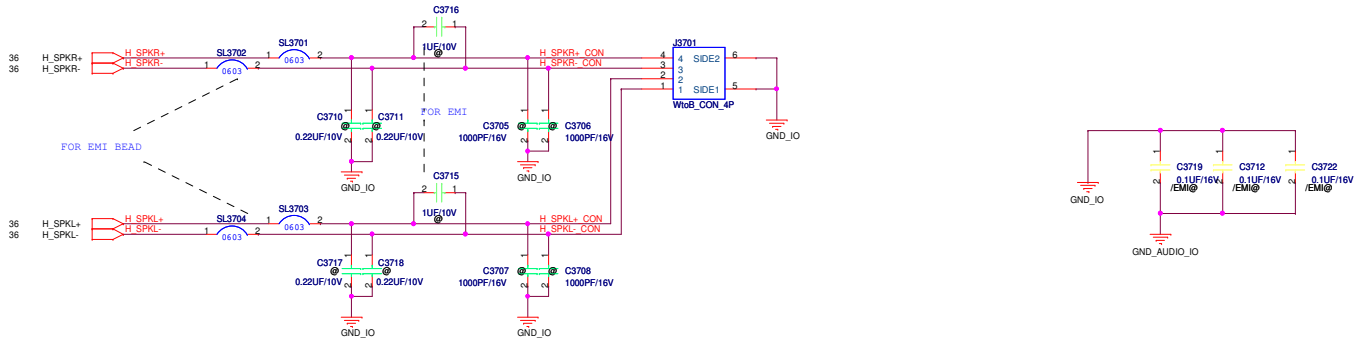
Ext MIC



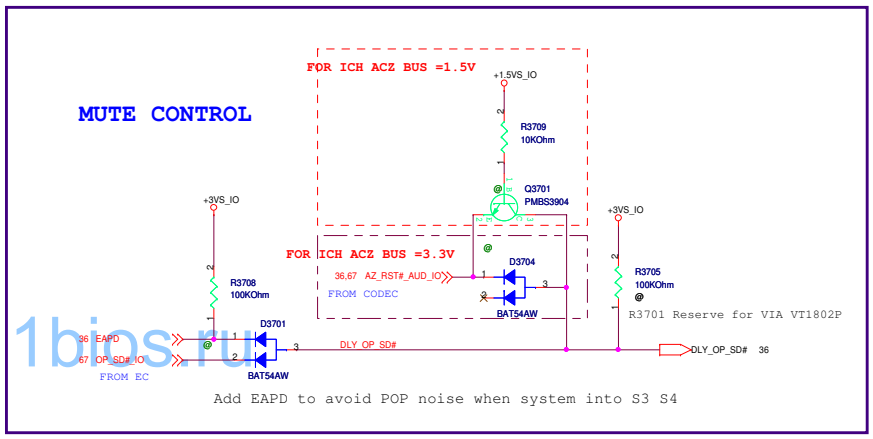
HP JACK



INT SPK



C3701~C3708 Reserve for VIA VT1802P



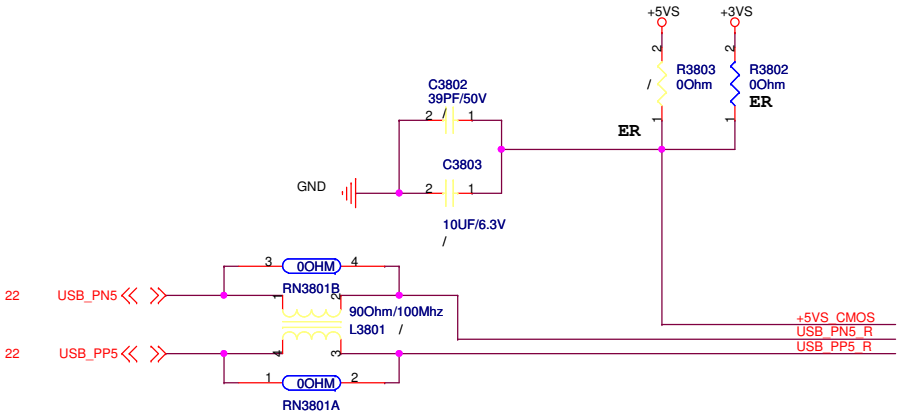
R3701 Reserve for VIA VT1802P

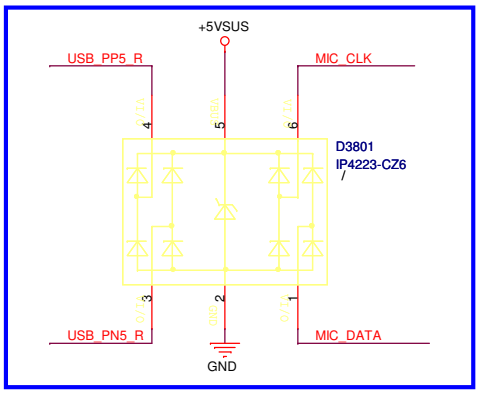
Add EAPD to avoid POP noise when system into S3 S4

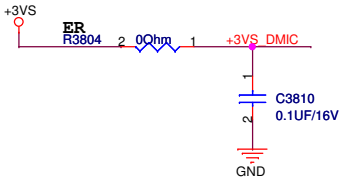
ASUSTEK COMPUTER INC	Title : ALC269-2 (I/O)	
	Engineer: Anndy_wang	
Size: Custom	Project Name: 1005P_IO	Rev: 1.3
Date: Monday, May 24, 2010	Sheet 37 of 97	

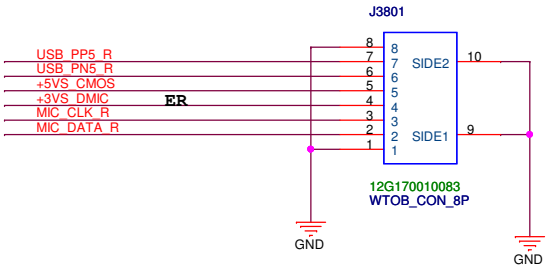
Camera Module & Mic.

R4501 and R4502 depend on CMOS module support.

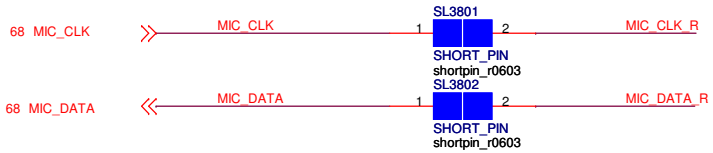


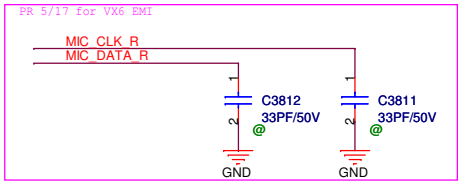






Int DMIC



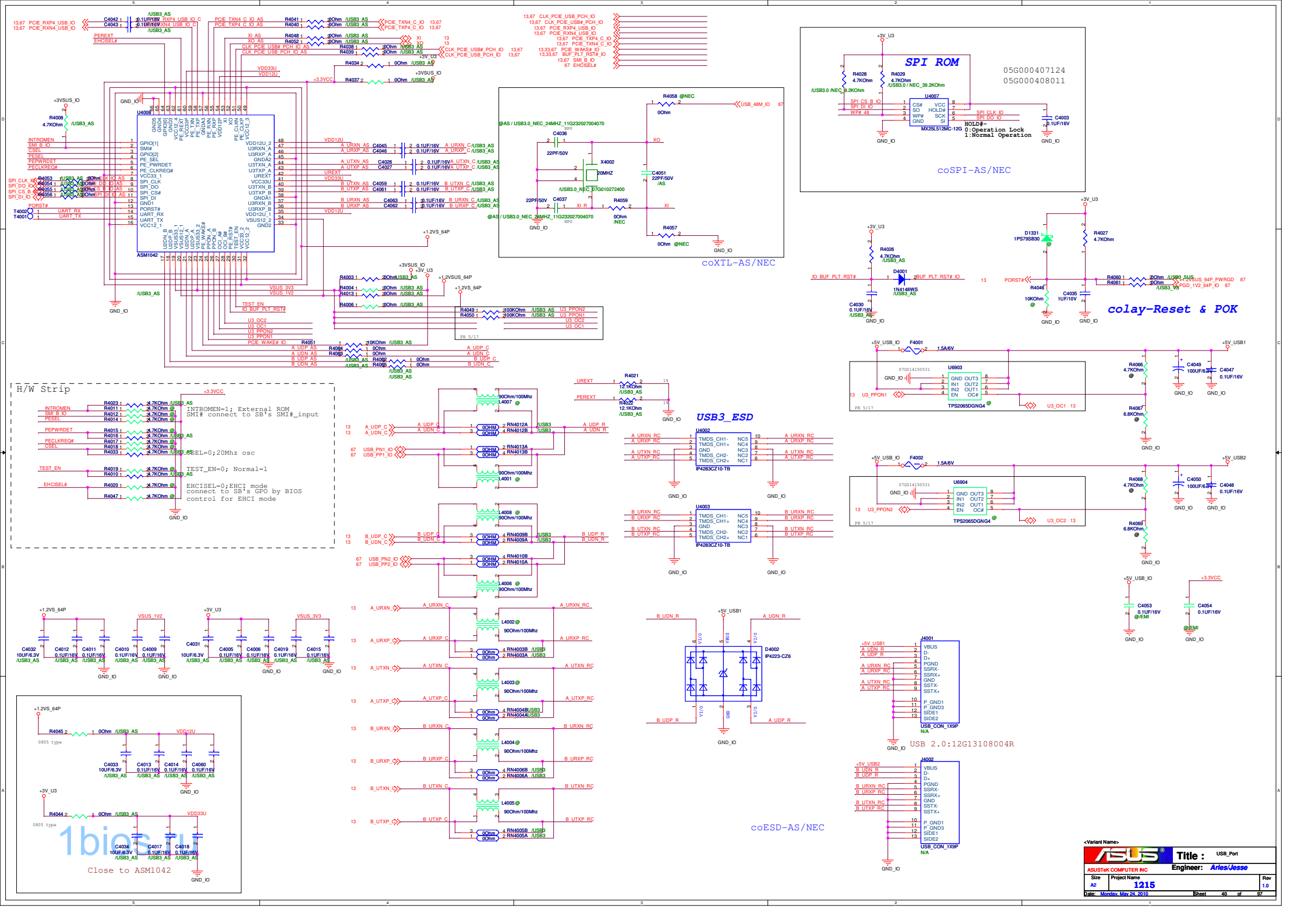


<Variant Name>

ASUSTeK COMPUTER INC	Title : I/O_SPK,INT MIC,CMOS	
	Engineer: Aries/Jesse	
Size: B	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 38 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title : IO_USB3.0_1***	
	Engineer: Aries/Jesse	
Size: C	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 39 of 97	


ASM1042
coSPI-AS/NEC
SPI ROM
05G000407124
05G000408011
MX25L512MC-12G
HOLD#-
0:Operation Lock
1:Normal Operation
coXTL-AS/NEC
colay-Reset & POK
USB3_ESD
coESD-AS/NEC
H/W Strip
INTROMEN=1; External ROM
SMI# connect to SB's SMI#_input
PESEL=0;20Mhz osc
TEST_EN=0; Normal=1
EHCISEL=0;EHCI mode
connect to SB's GPO by BIOS
control for EHCI mode
USB 2.0:12G13108004R
Close to ASM1042
1bios.ru
Title : USB_Port
Engineer: Aries/Jesse
ASUSTeK COMPUTER INC
Project Name 1215
Rev 1.0
Sheet 40 of 97

<Variant Name>

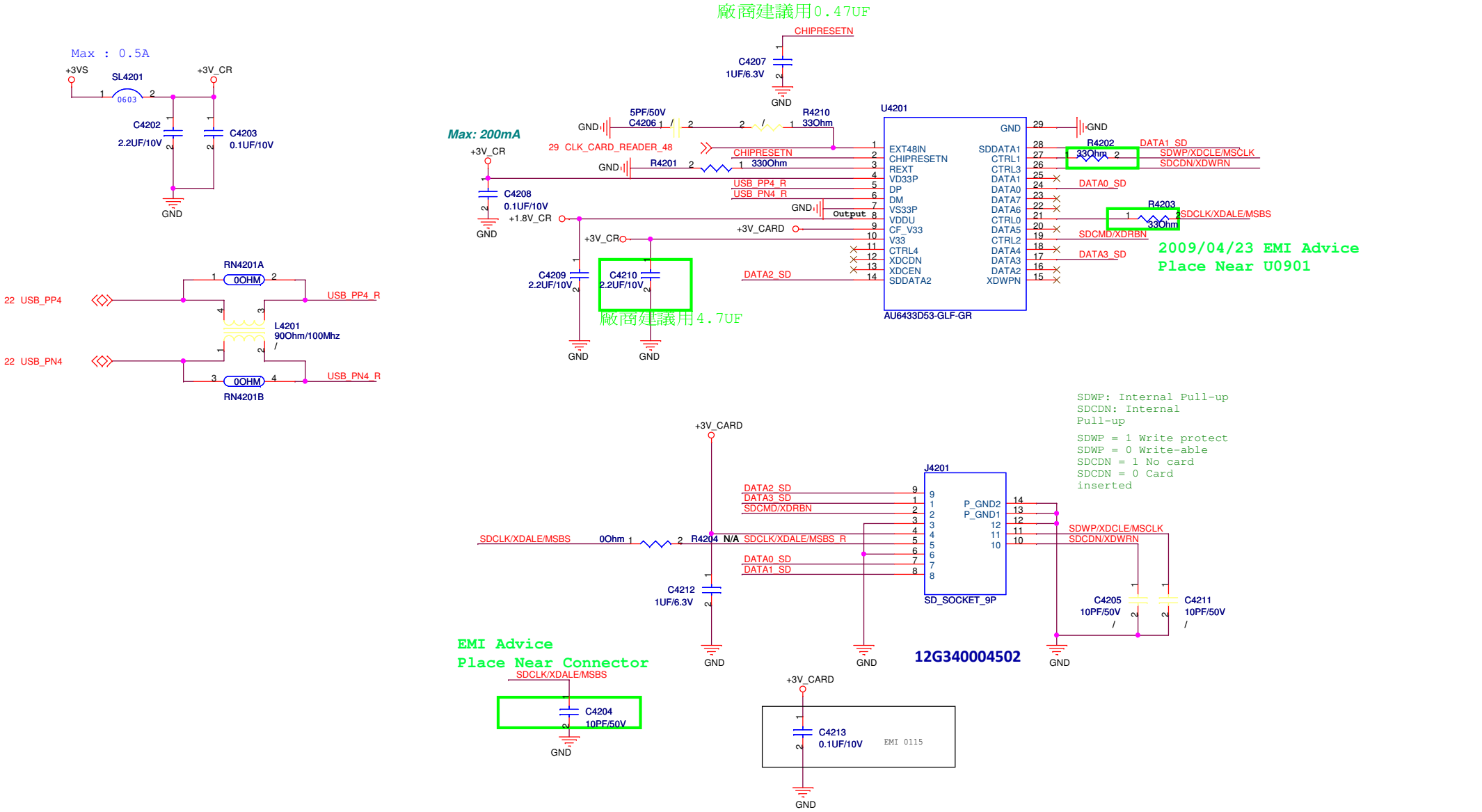
Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

Size	Project Name	Rev
A	UL20A	2.1

Date: Monday, May 24, 2010 Sheet 41 of 97



<Variant Name>

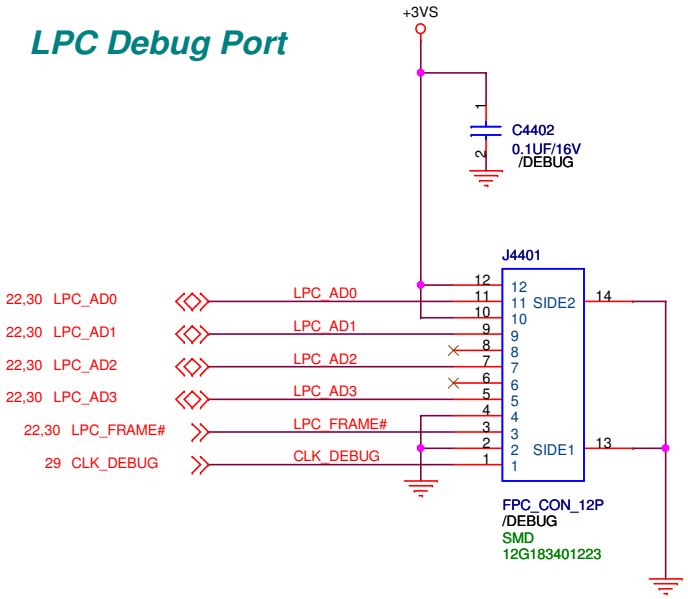
Title :	CARD READER AU6433
ASUSTeK COMPUTER INC	Engineer: Aries/Jesse
Size: B	Project Name: 1215
Rev: 1.0	
Date: Monday, May 24, 2010	Sheet 42 of 97

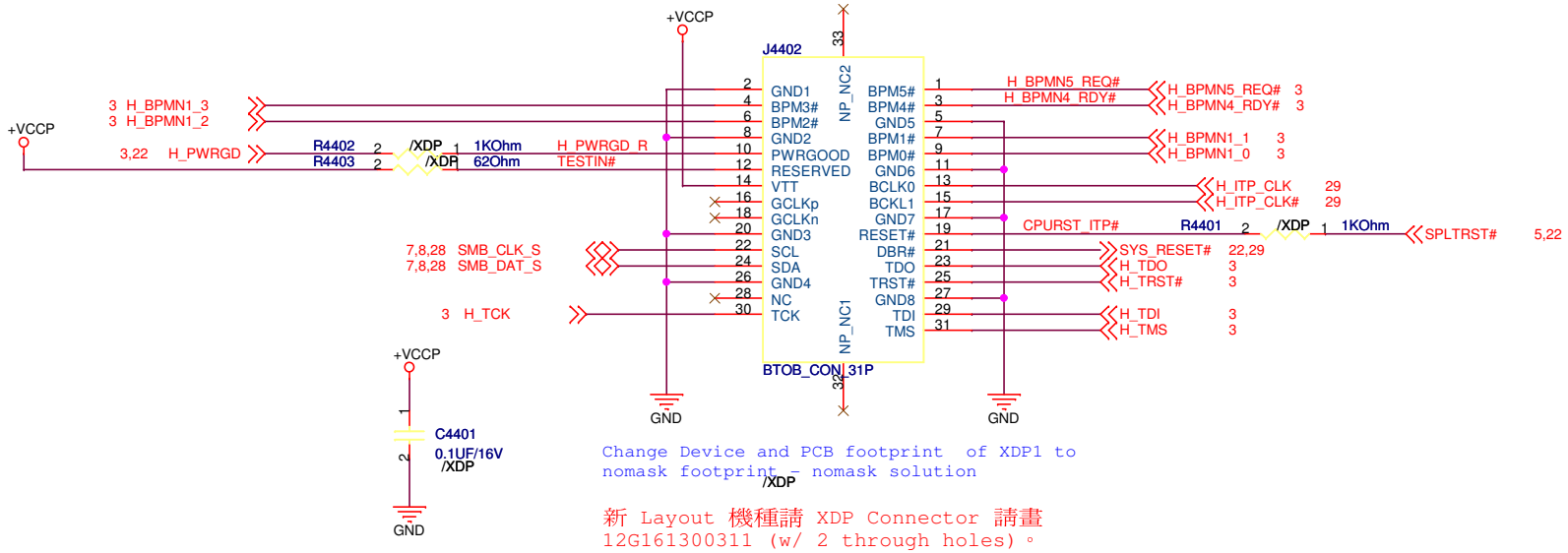
<Variant Name>

ASUSTeK COMPUTER INC	Title : CR EXPRESS CARD CONN	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.1
Date: Monday, May 24, 2010	Sheet 43 of 97	

LPC DEBUG PORT

LPC Debug Port





Change Device and PCB footprint of XDP1 to nomask footprint - nomask solution

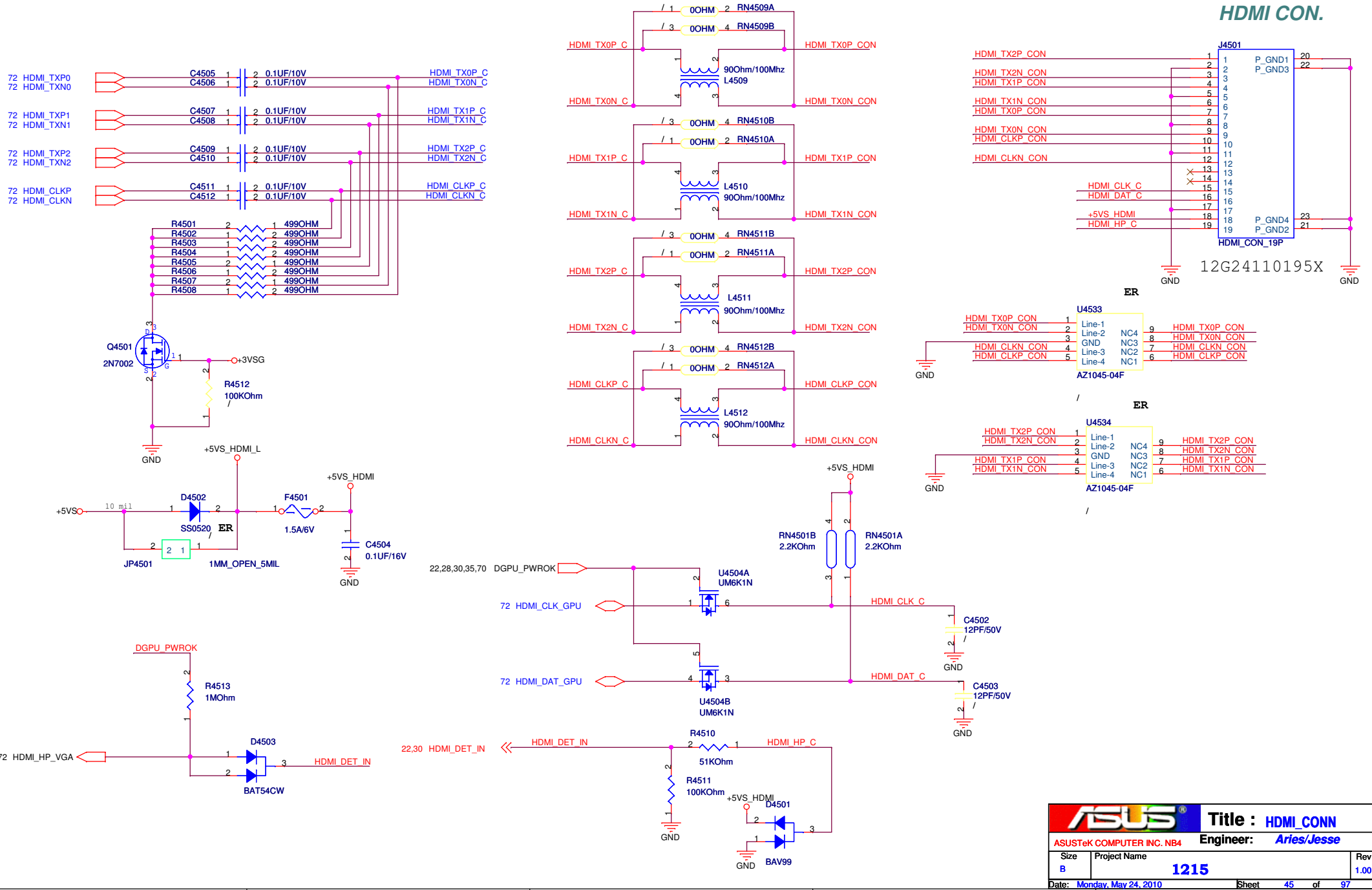
/XDP

新 Layout 機種請 XDP Connector 請畫 12G161300311 (w/ 2 through holes)。

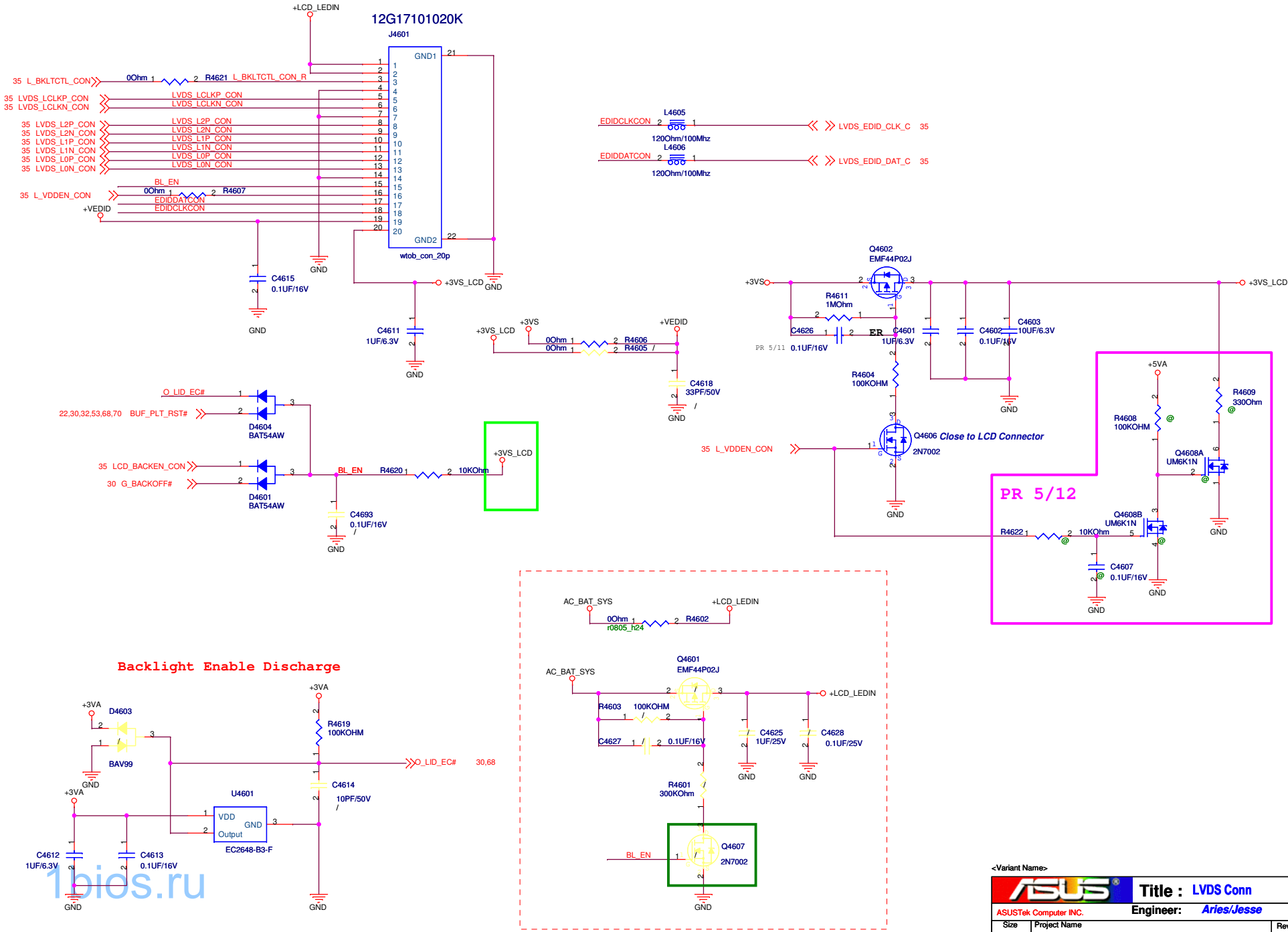
<Variant Name>

ASUSTeK COMPUTER INC	Title : BUG DEBUG PORT	
	Engineer: Aries/Jesse	
Size: Custom	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 44 of 97	

HDMI CON.



ASUSTeK COMPUTER INC. NB4	Title : HDMI_CONN		
	Engineer: Aries/Jesse		
Size: B	Project Name: 1215		Rev: 1.00
Date: Monday, May 24, 2010	Sheet 45 of 97		

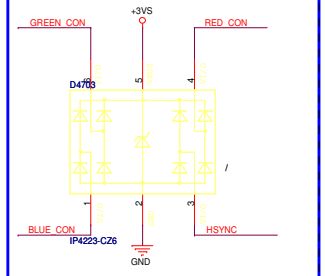


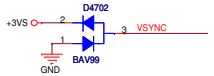
<Variant Name>

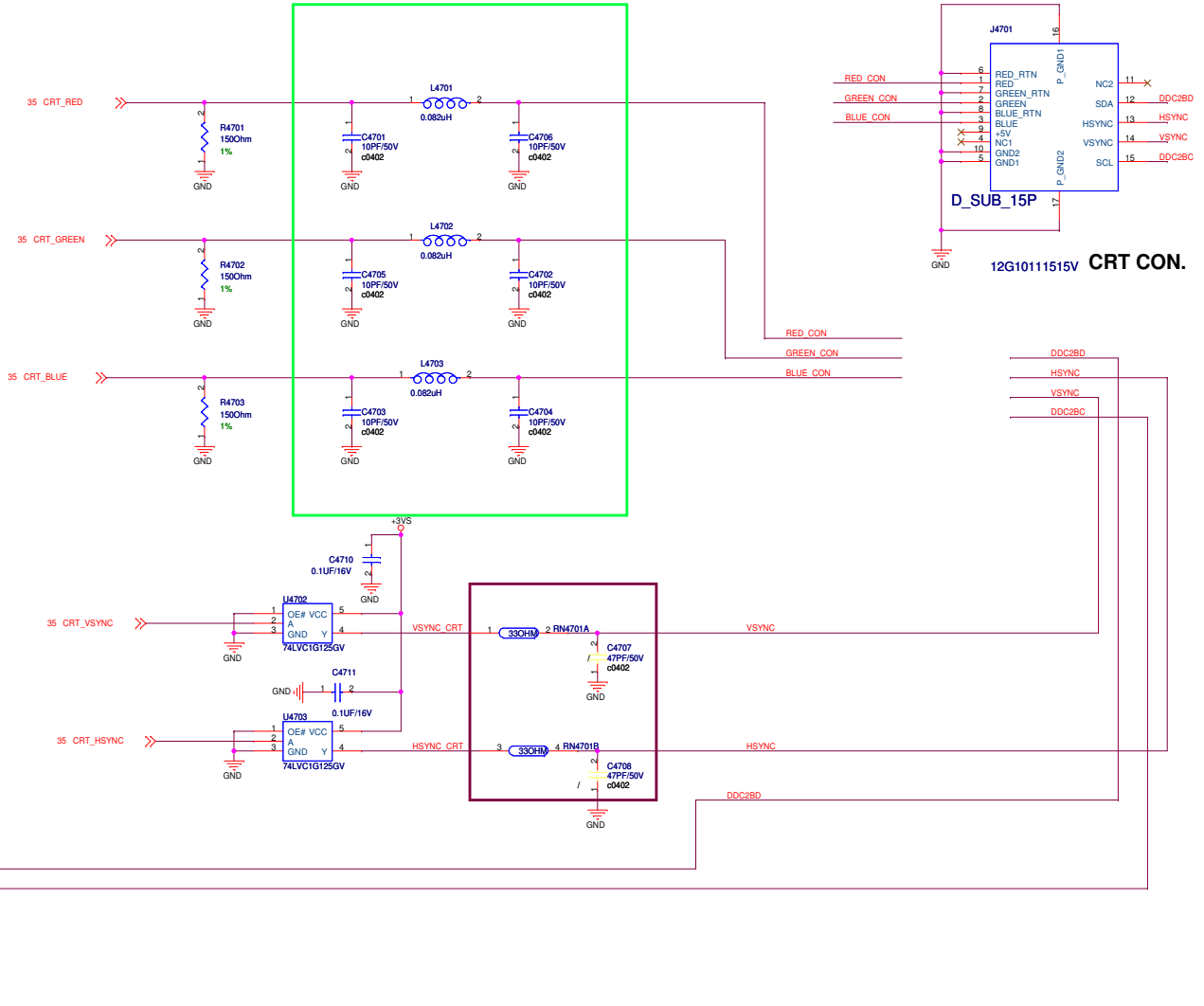
ASUSTek Computer INC.	Title : LVDS Conn	
	Engineer: Aries/Jesse	
Size: Custom	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 46 of 97	

Layout note: Near U7101

PLACE ESD Diodes near connector







12G10111515V **CRT CON.**

ASUSTeK COMPUTER INC.

Title : CRT_D-SUB

Engineer: Aries/Jesse

Size	Project Name	Rev
C	1215	1.0

Date: Monday, May 24, 2010 Sheet 47 of 97

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.1
Date: Monday, May 24, 2010	Sheet 48 of 97	

<Variant Name>

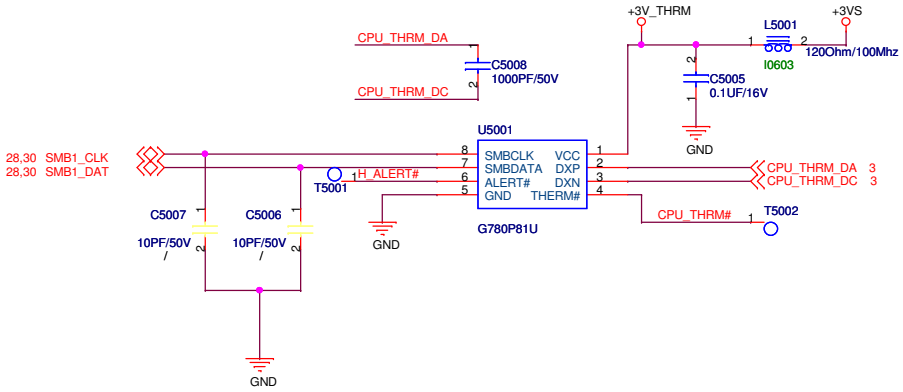
Title :

ASUSTeK COMPUTER INC

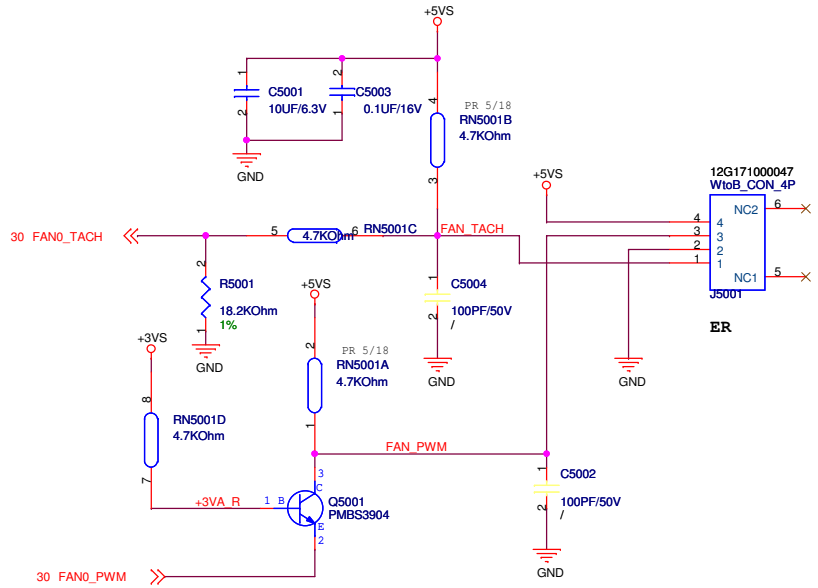
Engineer: Jerry Yu

Size	Project Name	Rev
A	UL20A	2.1

Date: Monday, May 24, 2010 Sheet 49 of 97



FAN CONN



<Variant Name>

Title : FAN THERMAL SENSOR FAN CONN

ASUSTeK COMPUTER INC

Engineer: Aries/Jesse

Size	Project Name	Rev
Custom	1215	1.0

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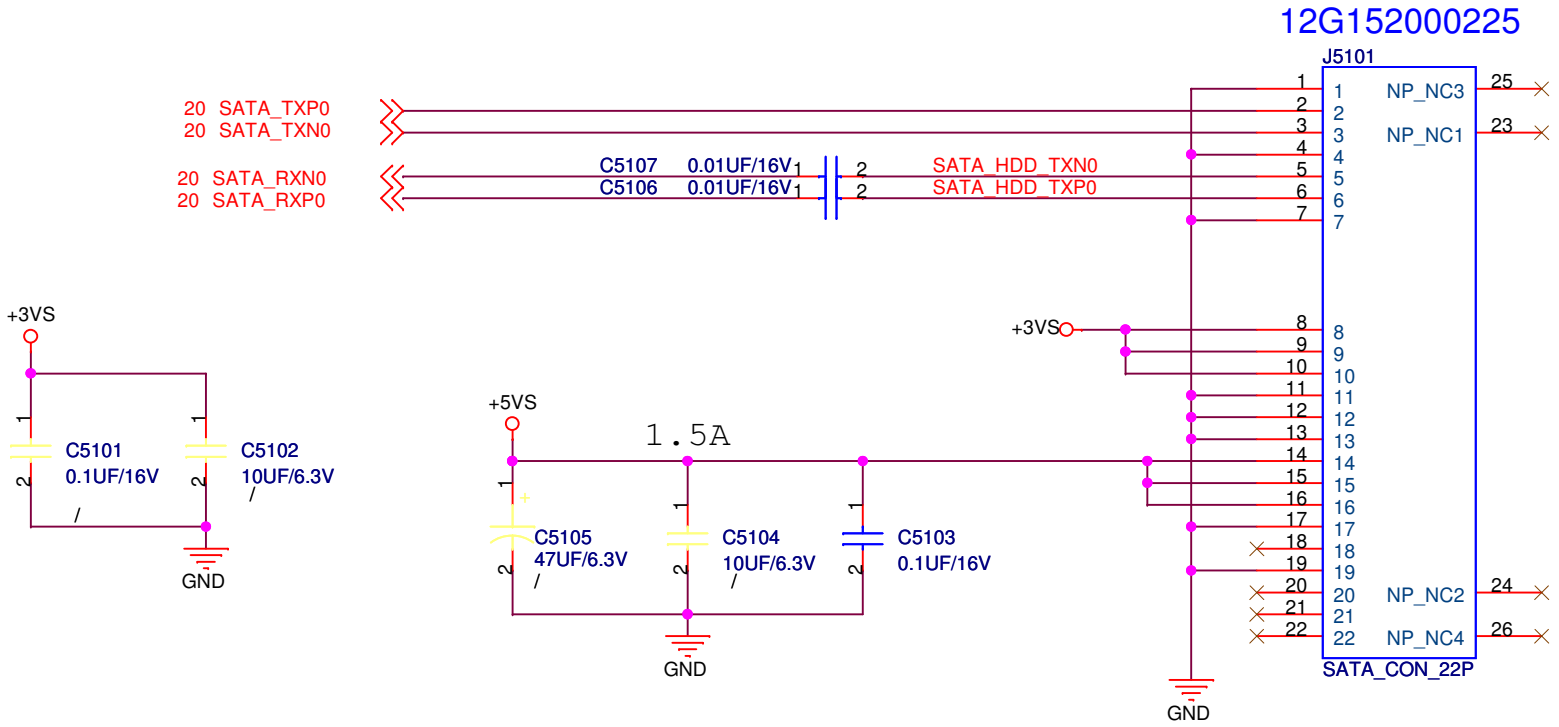
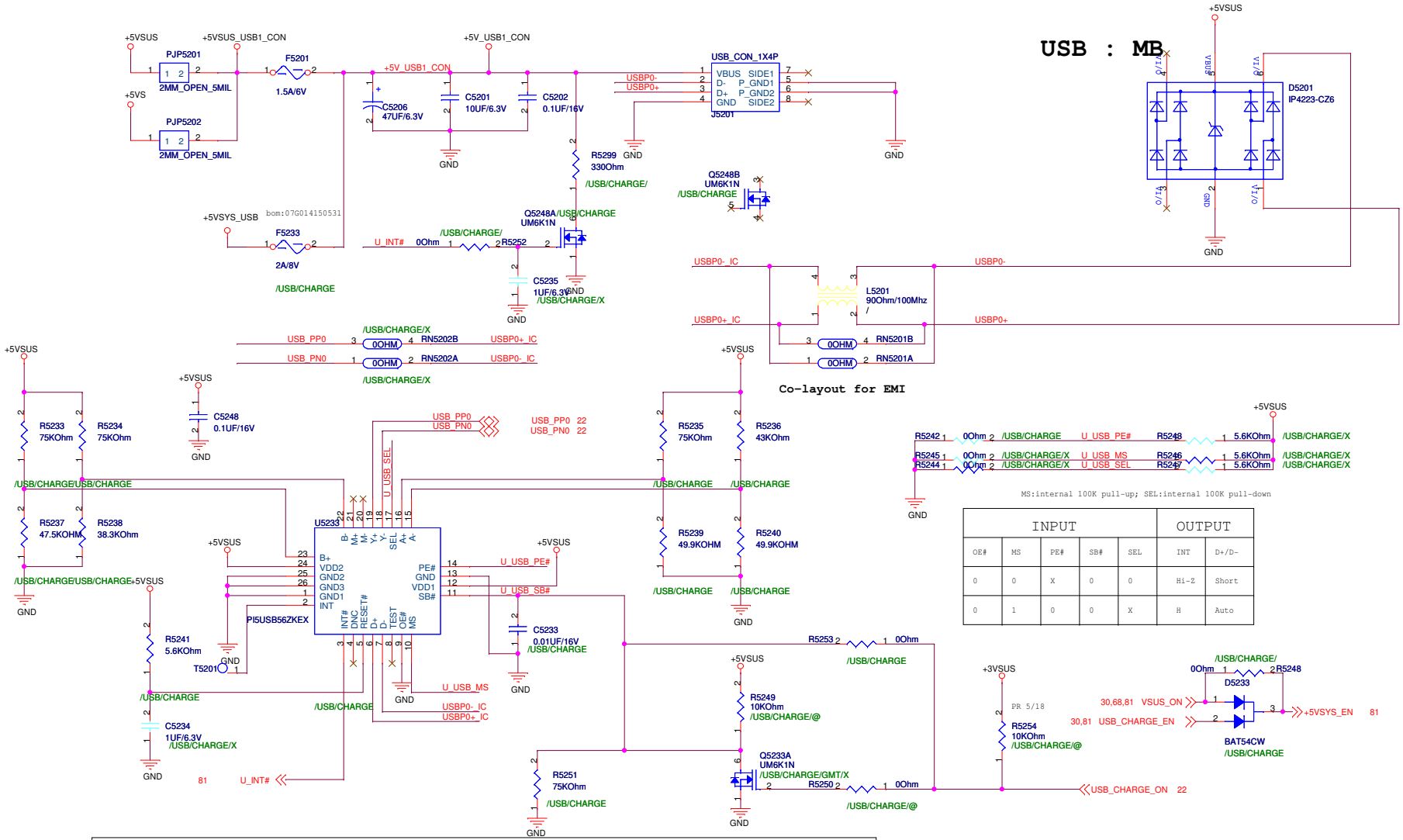
SATA HDD



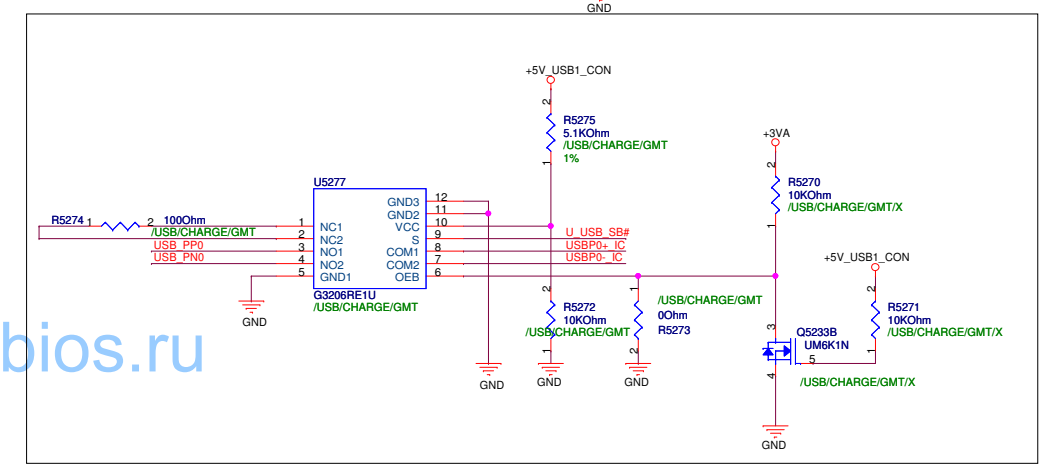
<Variant Name>

ASUSTeK COMPUTER INC	Title : XDD SATA HDD CONN	
	Engineer: Aries/Jesse	
Size: A	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 51 of 97	

USB : MB



ER



<Variant Name>

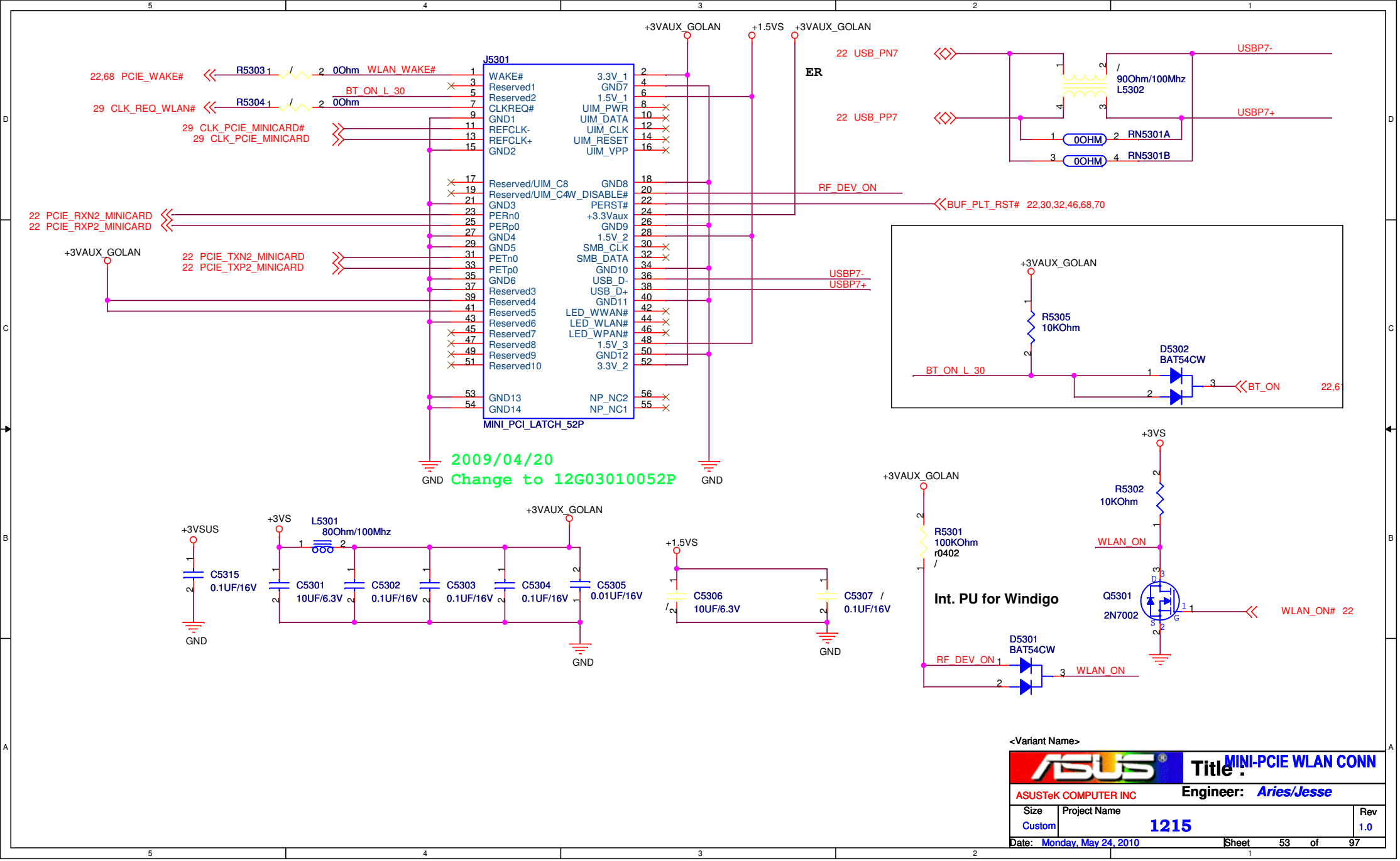
Title : USB 2.0 CONN*3

ASUSTeK COMPUTER INC

Engineer: Aries/Jesse

Size	Project Name	Rev
Custom	1215	1.0

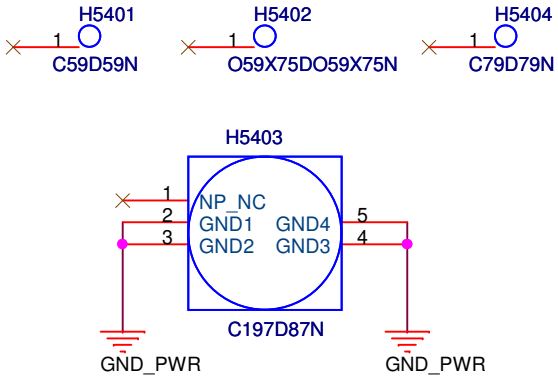
Date: Monday, May 24, 2010 Sheet 52 of 97



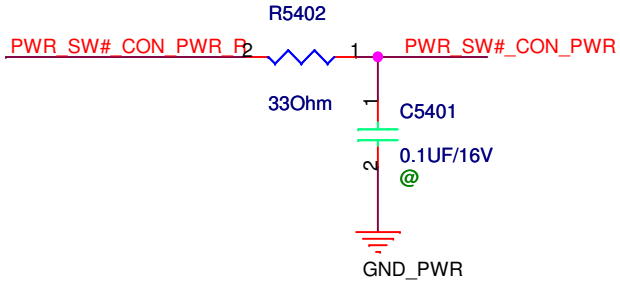
<Variant Name>

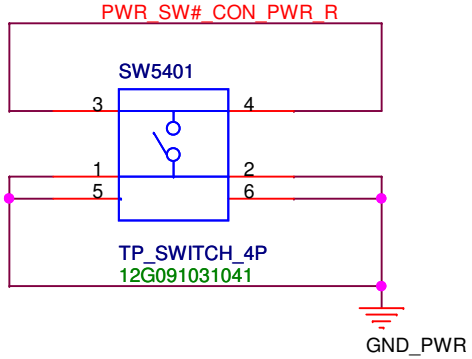
ASUSTeK COMPUTER INC	Title : MINI-PCIE WLAN CONN	
	Engineer: Aries/Jesse	
Size: Custom	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 53 of 97	

PWR SW

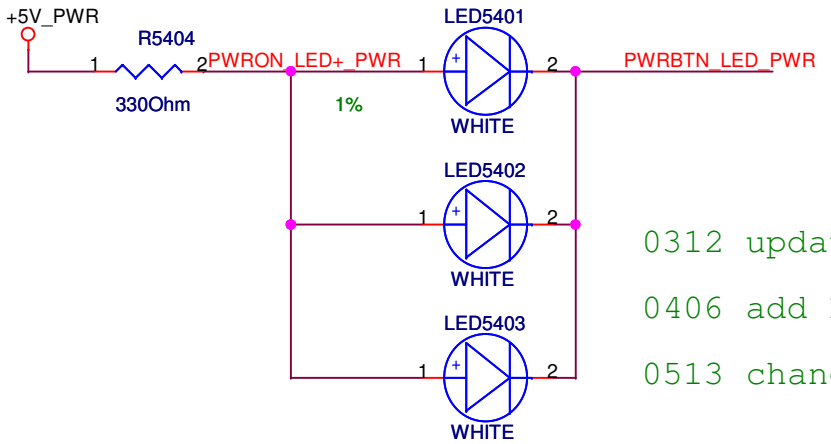


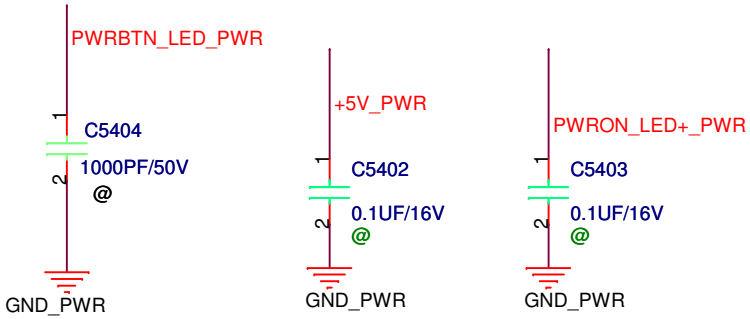
0510 revised hole





For POWER ON LED

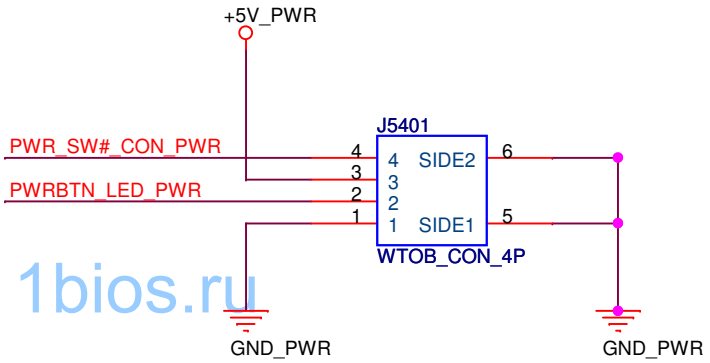




0312 update LED to 0603

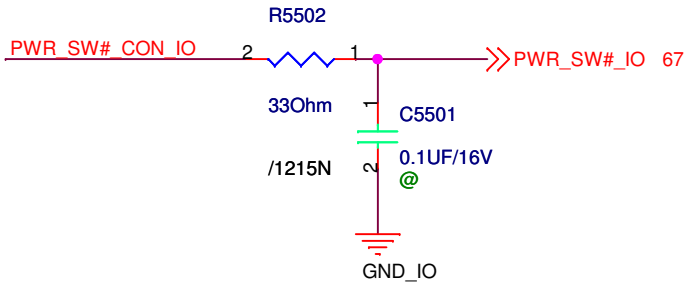
0406 add LED*3 (anderson)

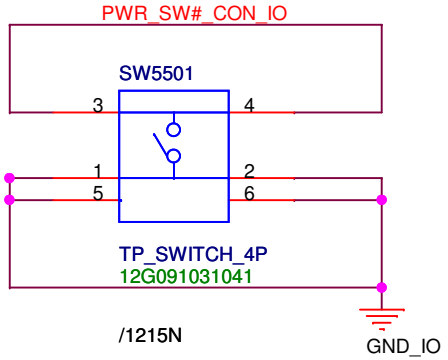
0513 change white LED



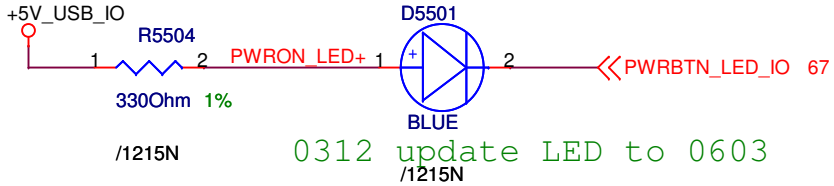
ASUSTEK COMPUTER INC	Title : PWR_BUTTON_LED	
	Engineer: Shangyu/Anderson	
Size: A	Project Name: VX6_PWR_BTN	Rev: 1.3
Date: Monday, May 24, 2010	Sheet 54 of 97	

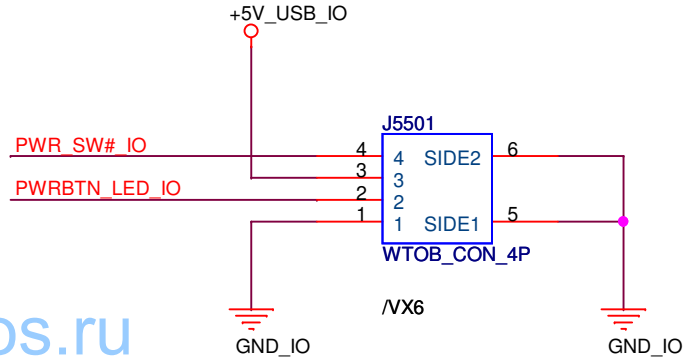
PWR SW





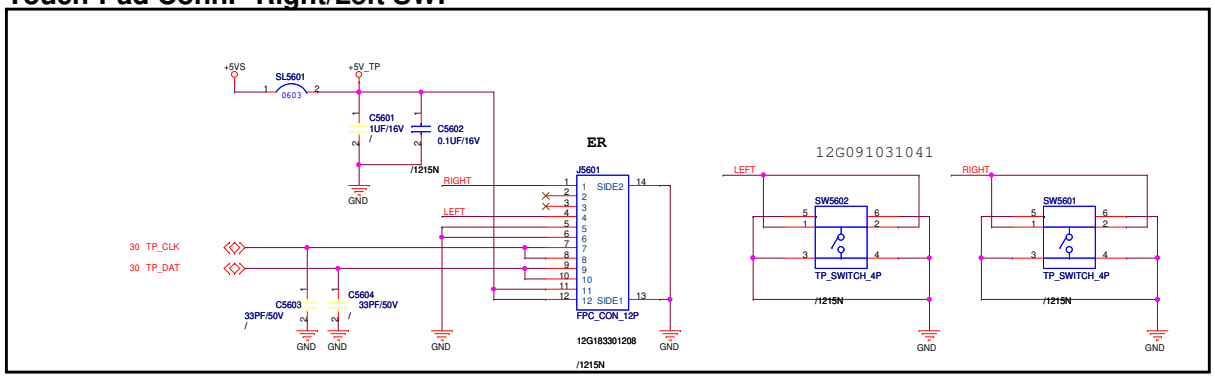
For POWER ON LED



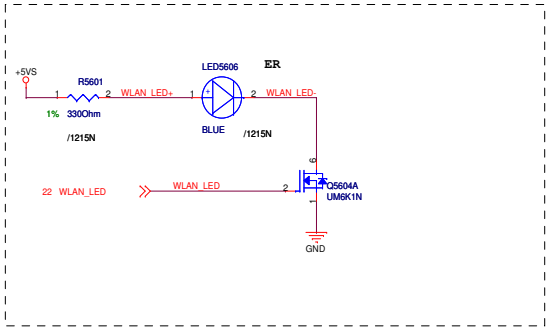


ASUSTEK COMPUTER INC	Title : PWR_BUTTON_LED	
	Engineer: Anndy_wang	
Size: A	Project Name: 1005P_IO	Rev: 1.3
Date: Monday, May 24, 2010	Sheet 55 of 97	

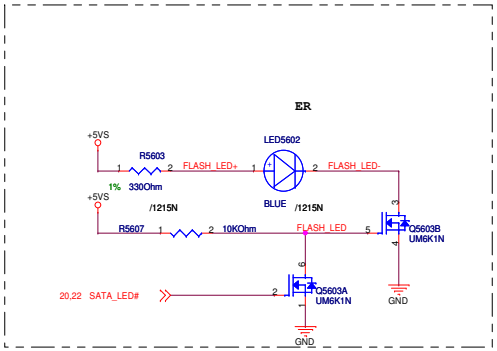
Touch-Pad Conn. Right/Left SW.



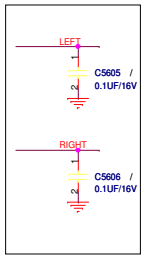
For WLAN LED



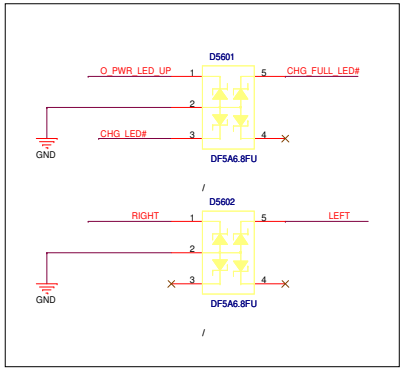
For IDE/FLASH LED



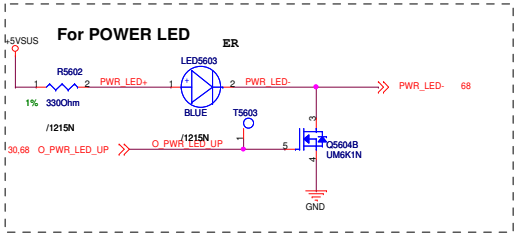
6/30 EMI near BTN



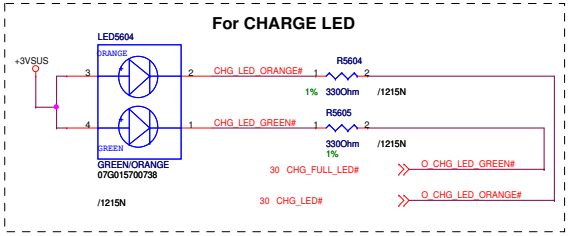
6/22 for ESD

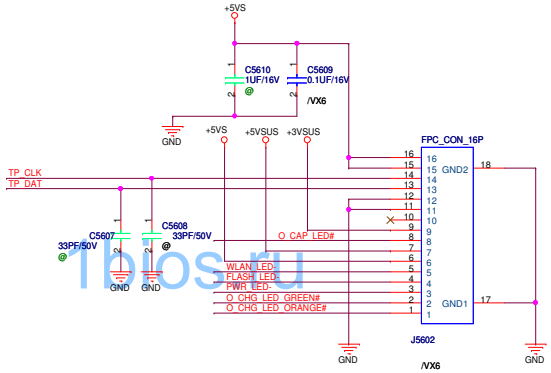


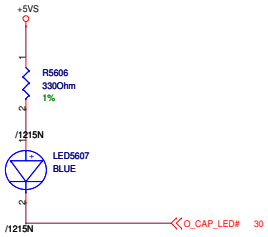
PWR LED



Charge LED

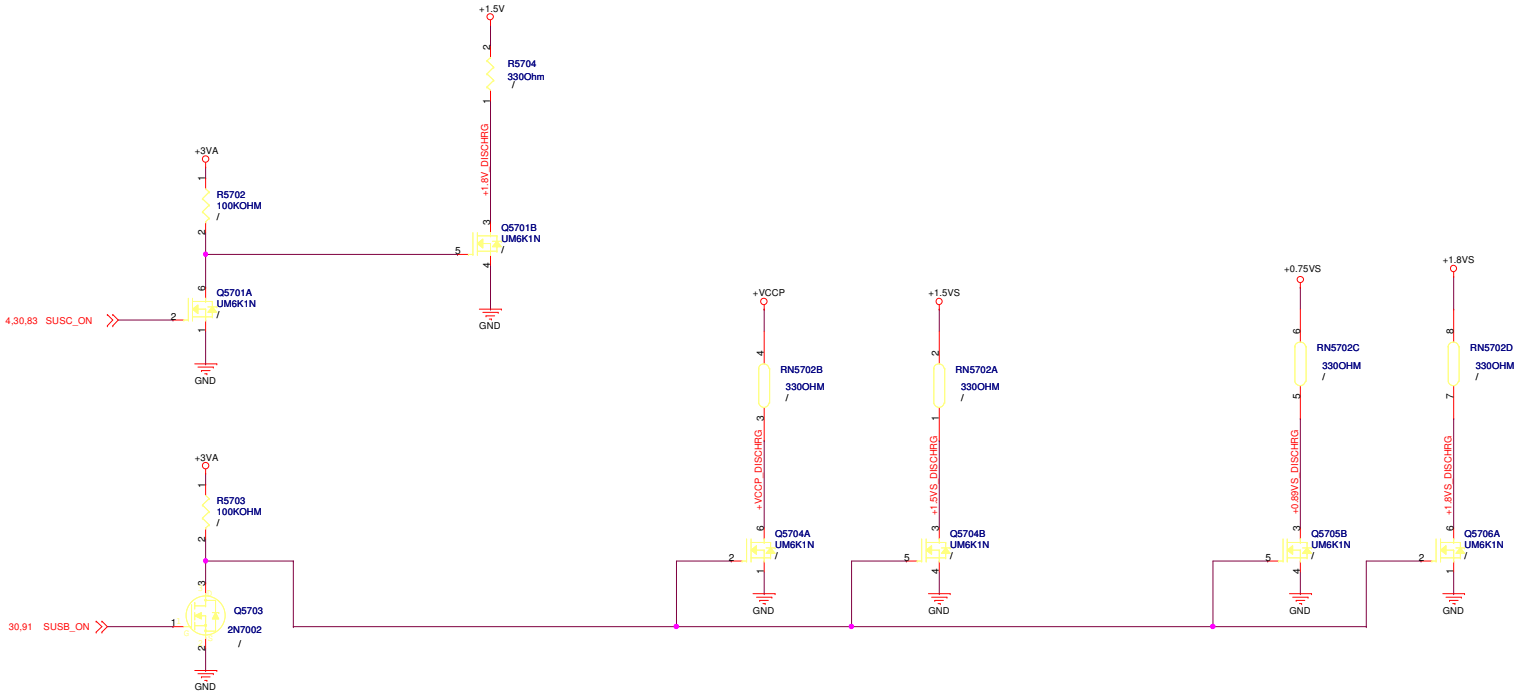






<Variant Name>

Title :	LED PWR LED FOC CONN
ASUSTeK COMPUTER INC	Engineer: Aries/Jesse
Size: C	Project Name: 1215
Rev: 1.0	
Date: Monday, May 24, 2010	Sheet 56 of 97



<Variant Name>

Title : Discharge

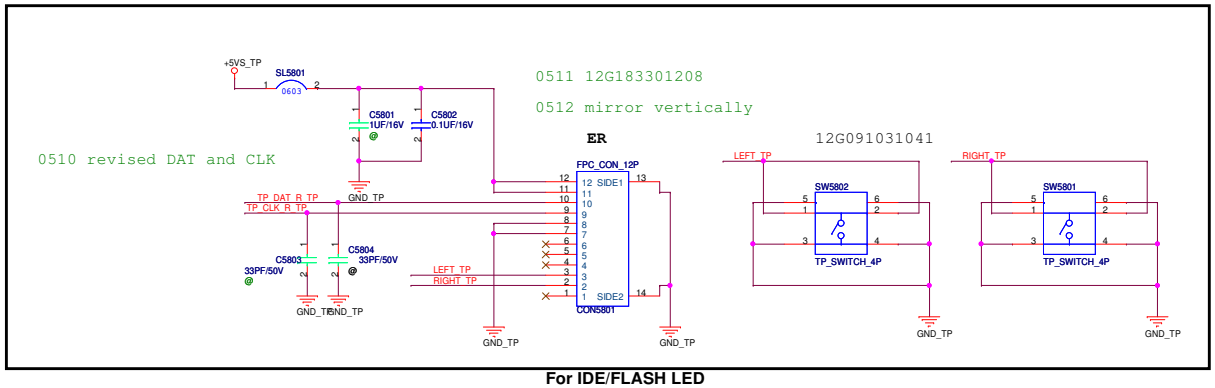
ASUSTek Computer INC.

Engineer: Aries/Jesse

Size	Project Name	Rev
Custom	1215	1.0

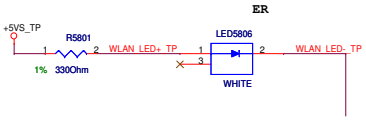
Date: Monday, May 24, 2010 Sheet 57 of 97

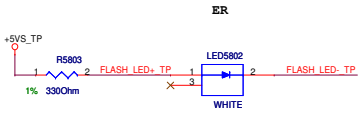
Touch-Pad Conn. Right/Left SW.



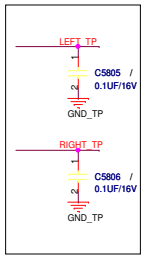
For IDE/FLASH LED

For WLAN LED

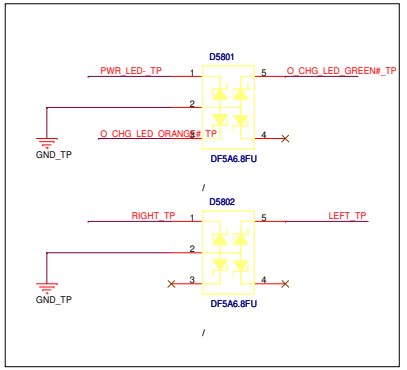




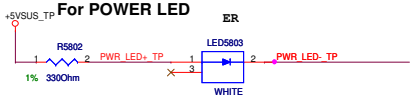
6/30 EMI near BTN



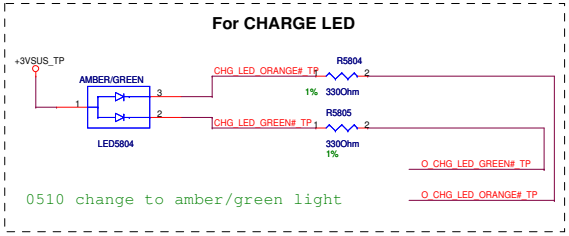
6/22 for ESD

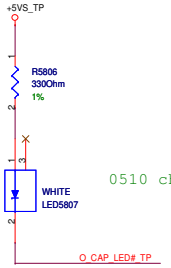


PWR LED

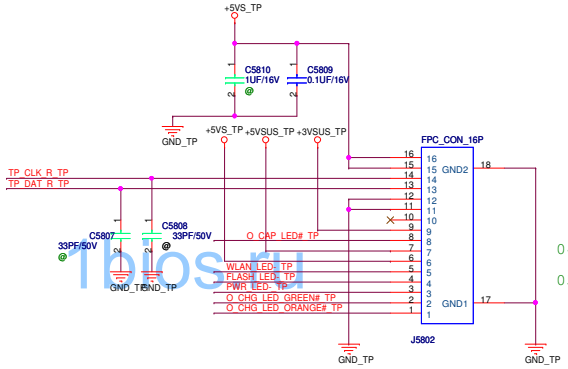


Charge LED



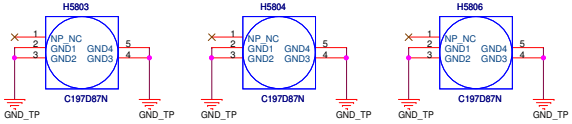


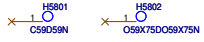
0510 change to white light



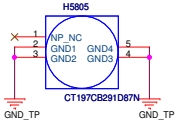
0406 mirror vertically (anderson)

0510 mirror vertically for positive/negative line





0510 revised hole



<Variant Name>

ASUSTeK COMPUTER INC

Title : LED PWR LED FOC CONN

Engineer: Shangyu/Anderson

Size	Project Name	Rev
C	VX6_TP	1.0

Date: Monday, May 24, 2010 Sheet 58 of 97

<Variant Name>

Title :

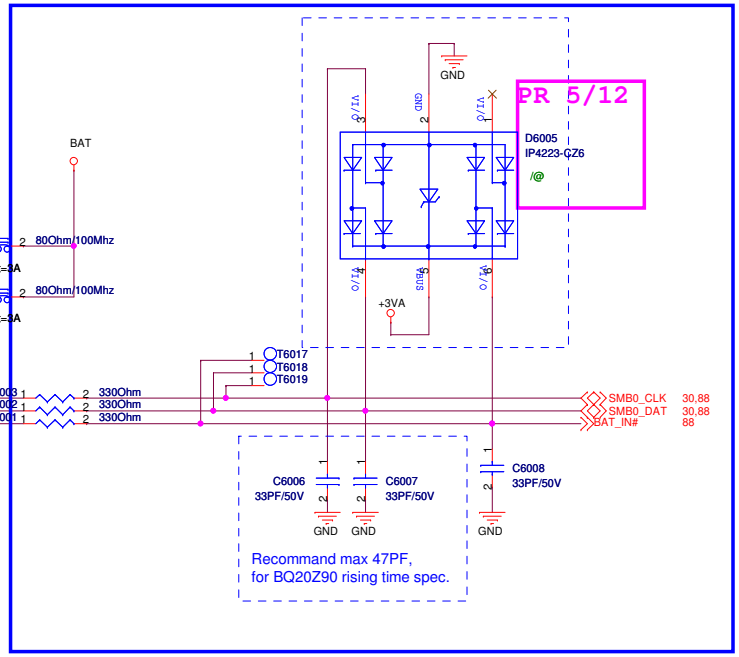
ASUSTeK COMPUTER INC

Engineer: Jerry Yu

Size	Project Name	Rev
A	UL20A	2.1

Date: Monday, May 24, 2010 Sheet 59 of 97

Battery Connector

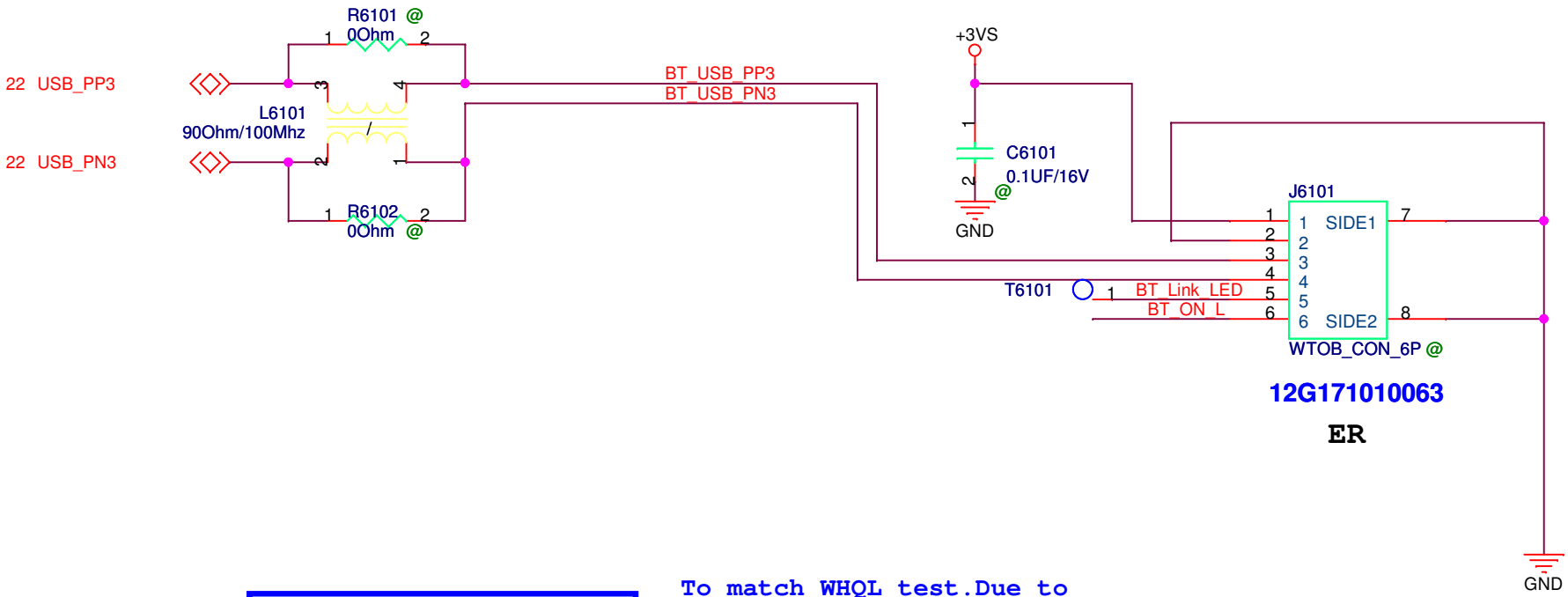


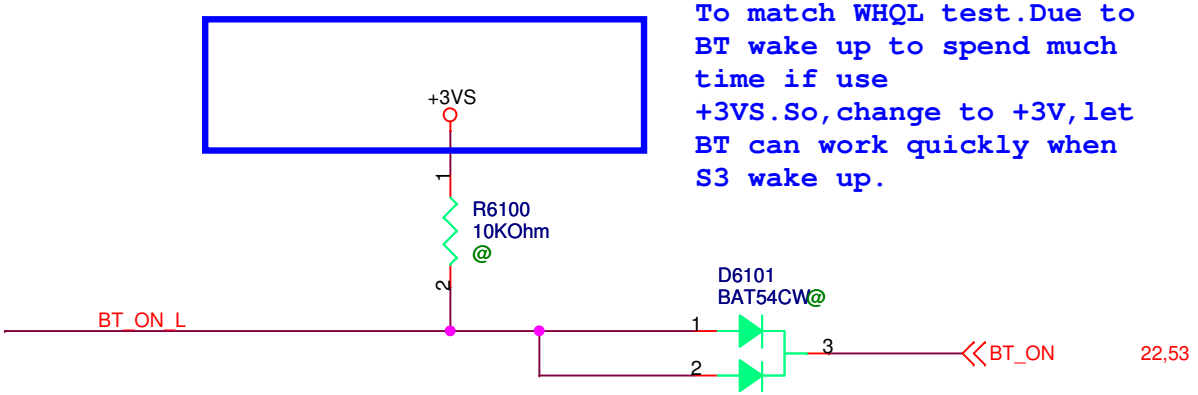
Total count: 11 pcs

081111 -> 090604:
1. Change D6005 from DF5A6.8FU to IP4223-CZ6 for cost down and integration.

ASUSTeK COMPUTER INC. NB1	Title : DC_DC & BAT IN	
	Engineer: Aries/Jesse	
Size: Custom	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 60 of 97	

BLUETOOTH CONNECTOR





To match WHQL test.Due to BT wake up to spend much time if use +3VS.So,change to +3V,let BT can work quickly when S3 wake up.

ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: Aries/Jesse	
Size: Custom	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 61 of 97	

<Variant Name>

Title : TPM

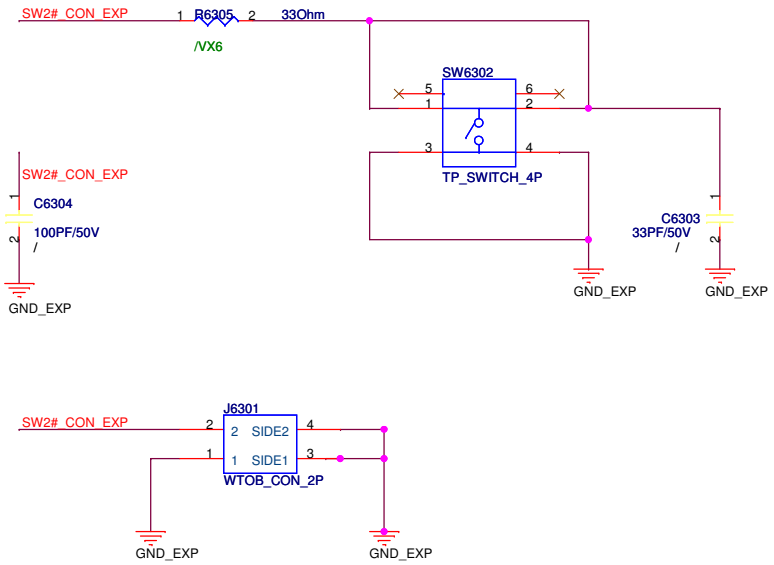
ASUSTeK COMPUTER INC

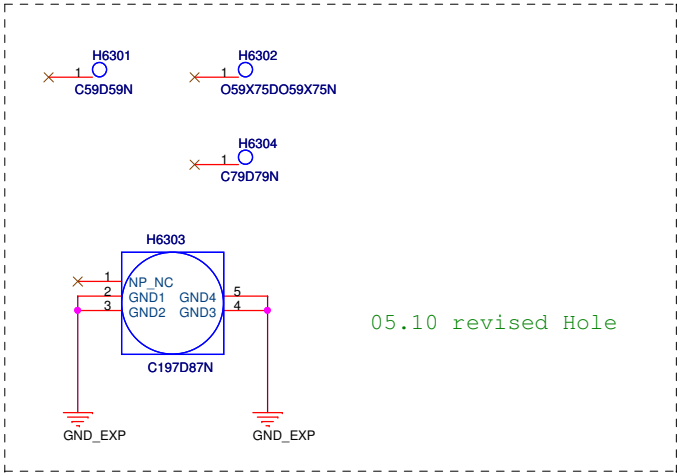
Engineer: Jerry Yu

Size	Project Name	Rev
A	UL20A	2.1

Date: Monday, May 24, 2010 Sheet 62 of 97

Express gate





<Variant Name>

CMO CMOS CAMERA

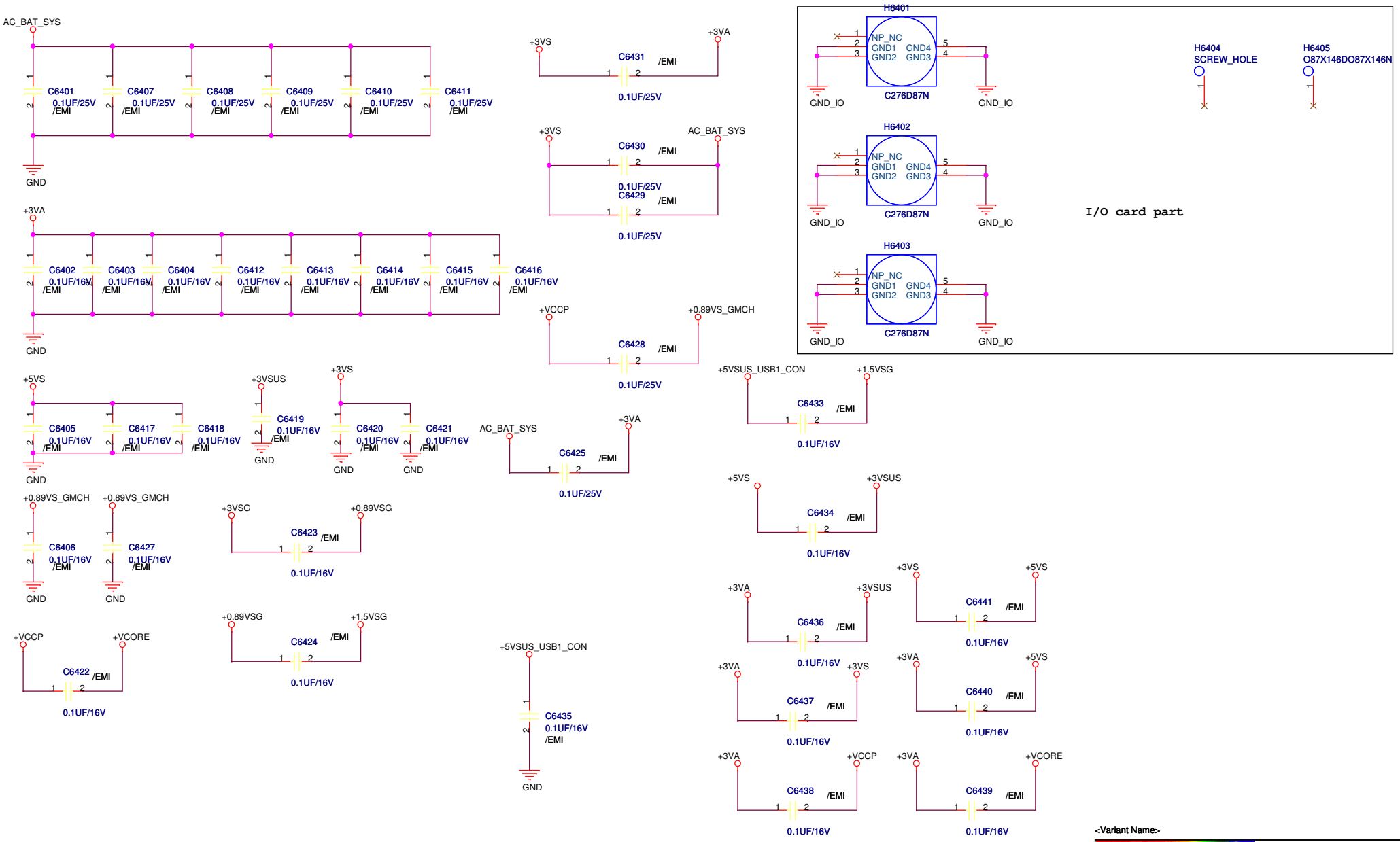
ASUSTeK COMPUTER INC

Title :

Engineer: Shangyu/Anderson

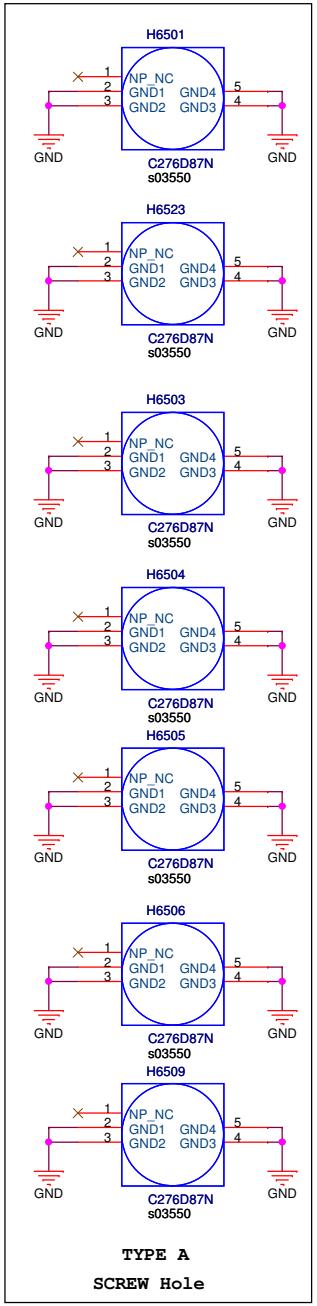
Size	Project Name	Rev
B	VX6_EXP	1.0

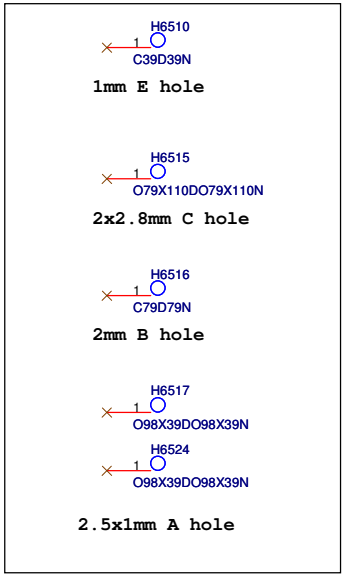
Date: Monday, May 24, 2010 Sheet 63 of 97

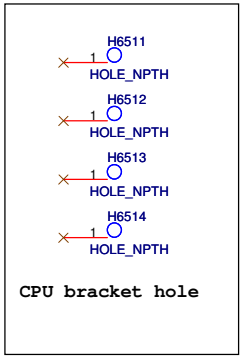


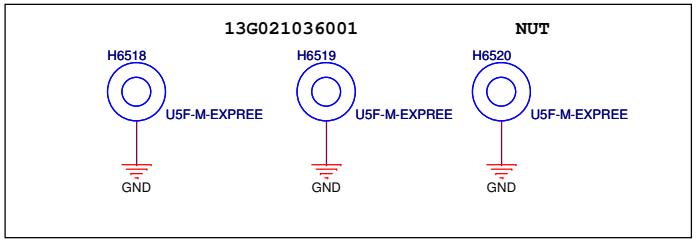
<Variant Name>

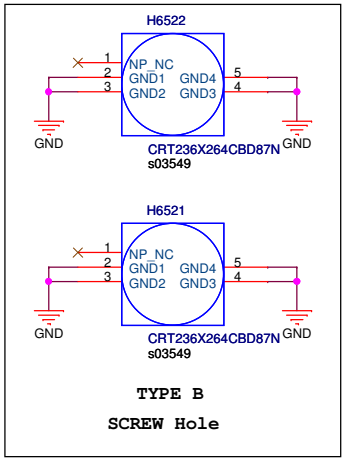
ASUSTeK COMPUTER INC	Title : EMI_CAP	
	Engineer: Aries/Jesse	
Size: B	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 64 of 97	





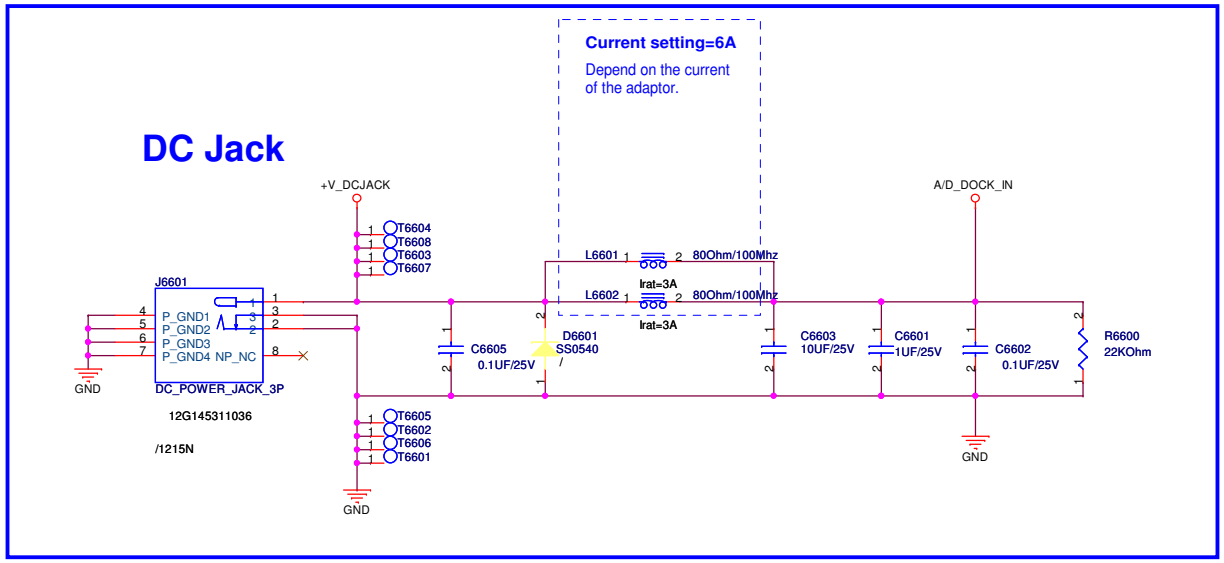


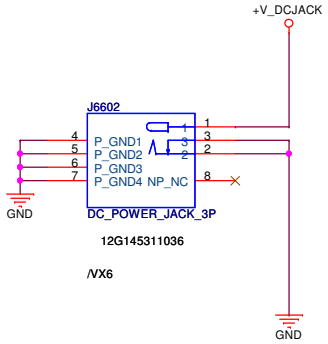




<variant_name>

ASUSTek Computer INC.	Title : Srew Hole	
	Engineer: Aries/Jesse	
Size: B	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 65 of 97	





<Variant Name>

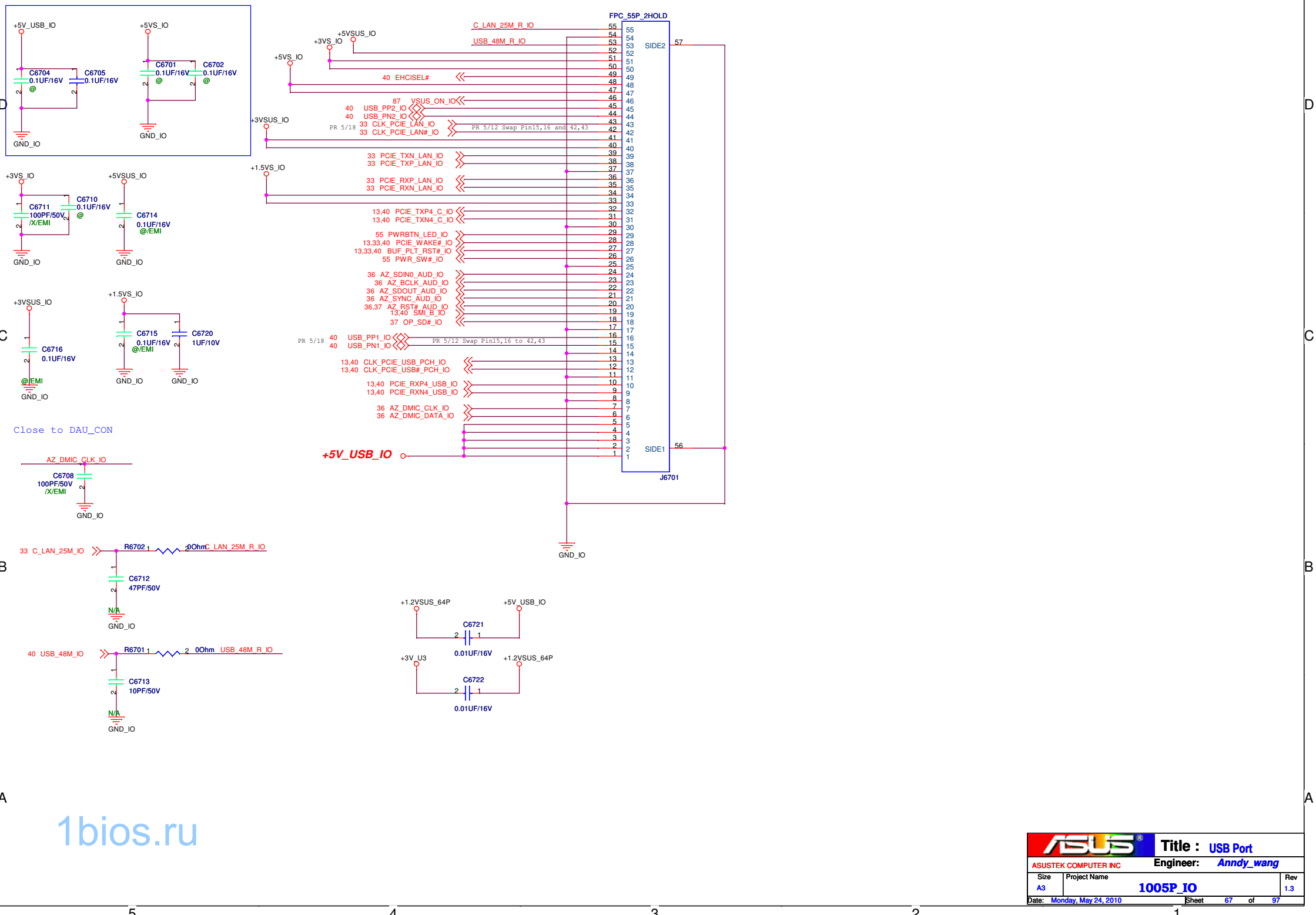
ASUSTeK COMPUTER INC

Title : RTC_DC CON

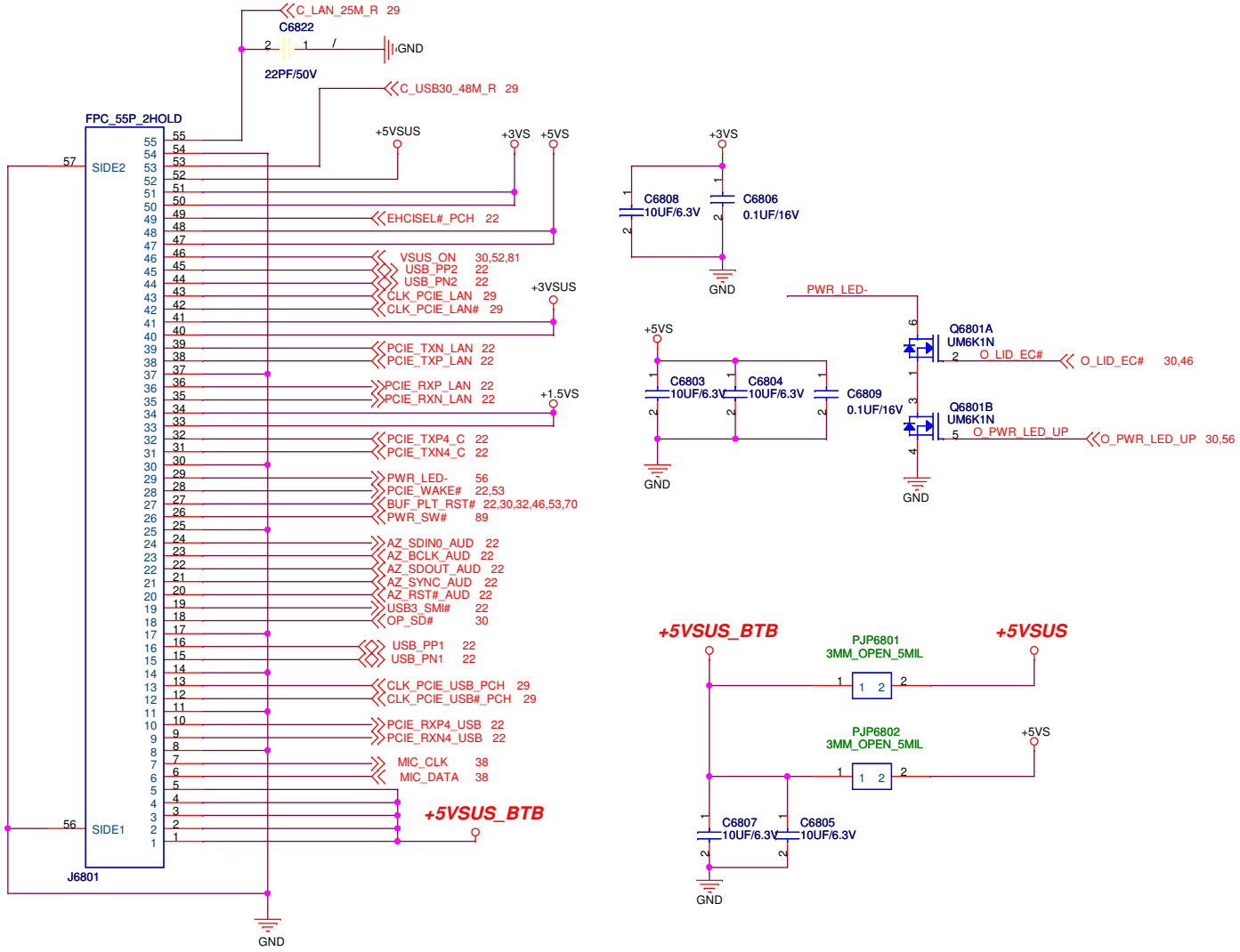
Engineer: Aries/Jesse

Size	Project Name	Rev
Custom	1215	1.0

Date: Monday, May 24, 2010 Sheet 66 of 97



ASUSTEK COMPUTER INC	Title : USB Port	
	Engineer: Anndy_wang	
Size: A3	Project Name: 1005P_IO	Rev: 1.3
Date: Monday, May 24, 2010	Sheet 67 of 97	



<Variant Name>

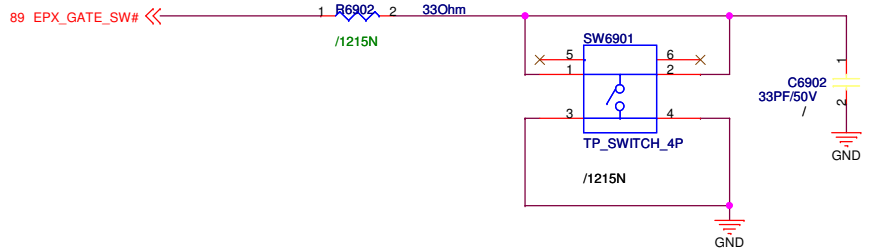
ASUSTeK COMPUTER INC

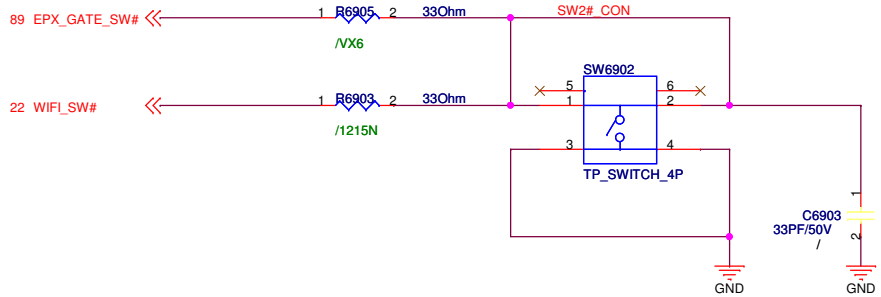
Title : B TO B CONN

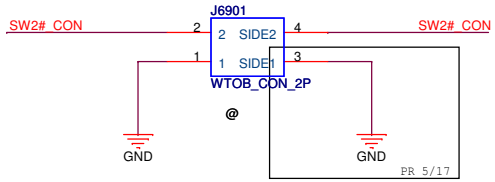
Engineer: Ariee/Jesse

Size	Project Name	Rev
B	1215	1.0

Date: Monday, May 24, 2010 Sheet 68 of 97







<Variant Name>

CMO CMOS CAMERA

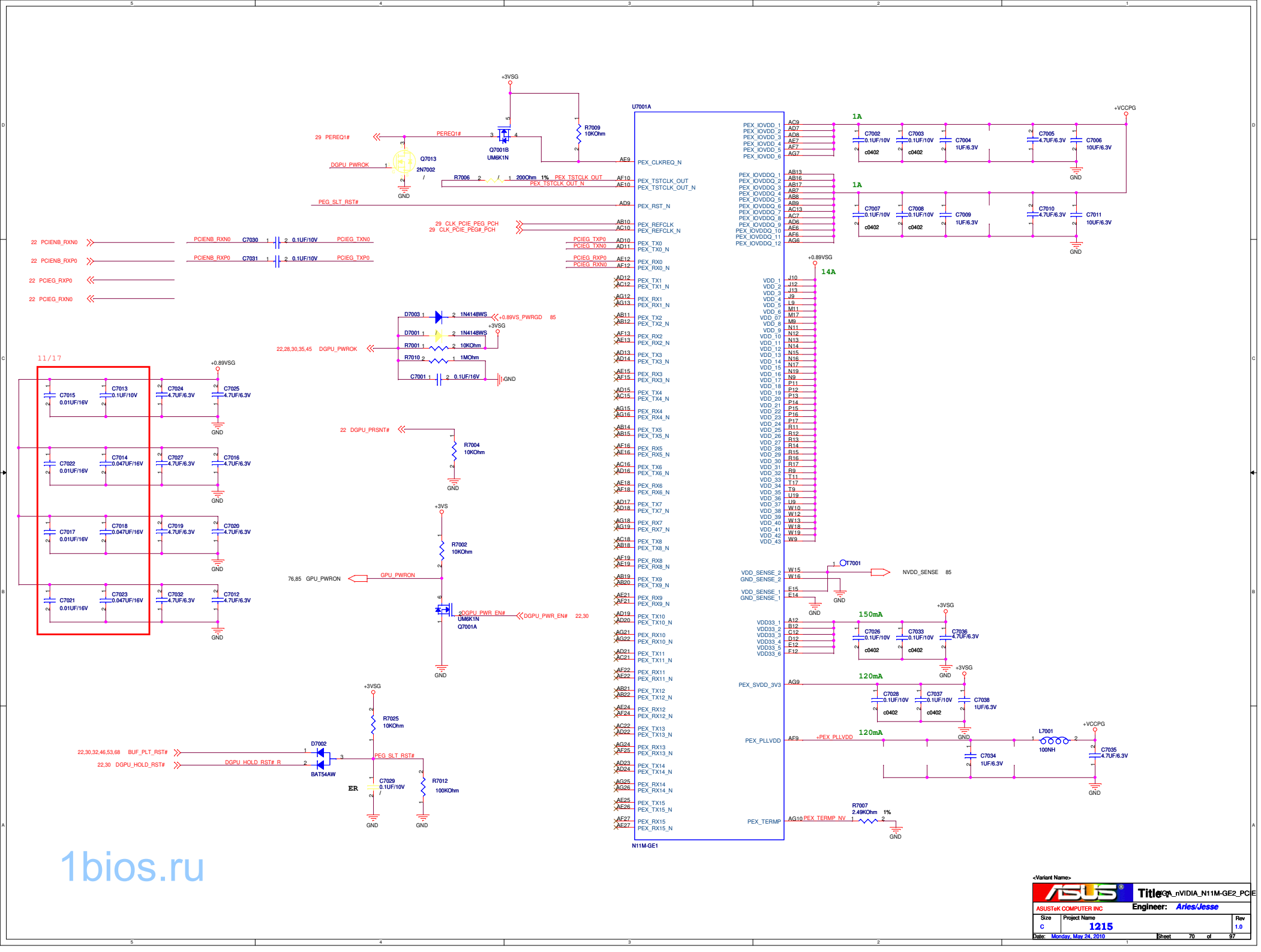
ASUSTeK COMPUTER INC

Title :

Engineer: Aries/Jesse

Size	Project Name	Rev
B	1215	1.0

Date: Monday, May 24, 2010 Sheet 69 of 97



<Variant Name>

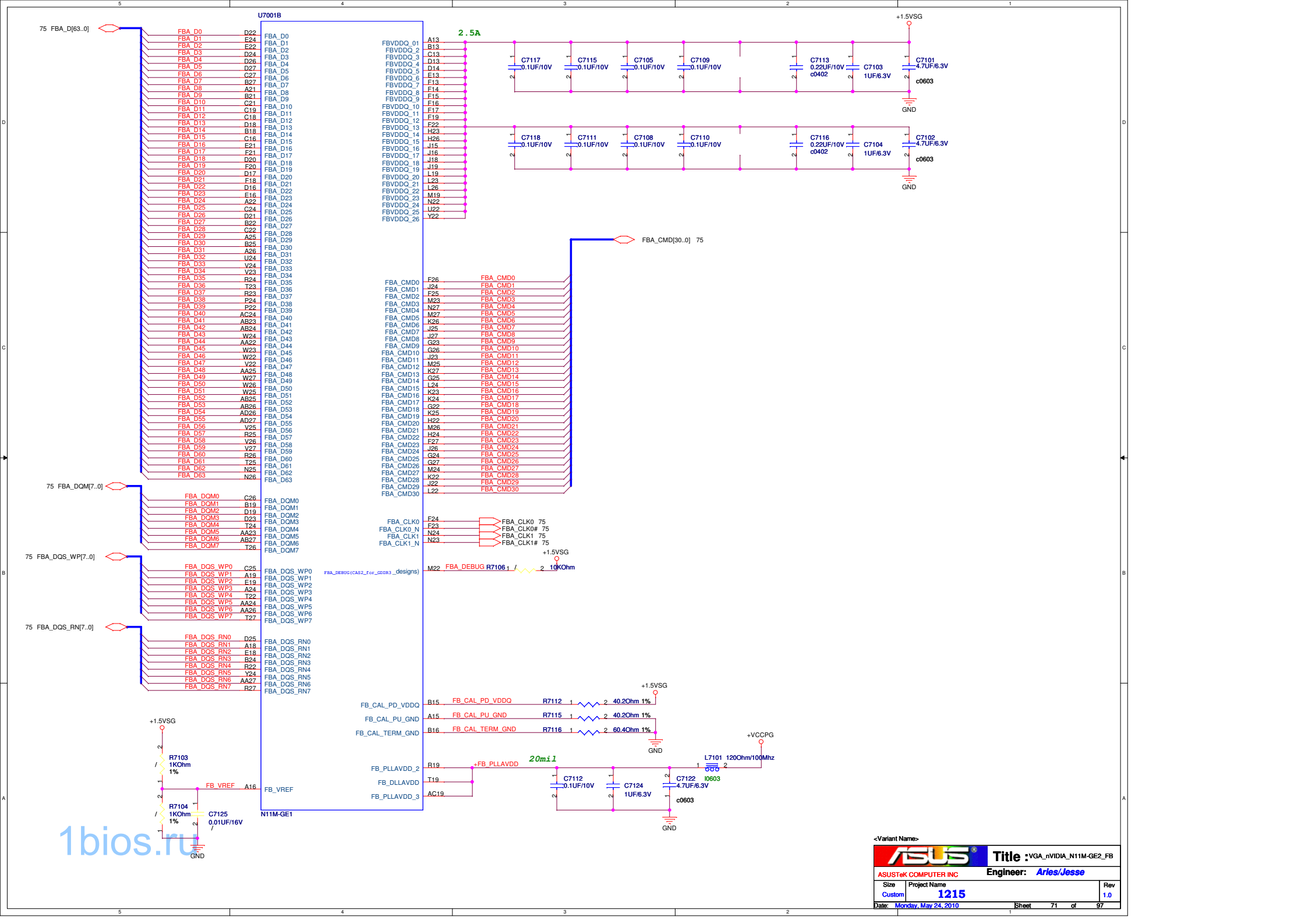
ASUSTeK COMPUTER INC

Title: SCH_nVIDIA_N11M-GE2_PCI-E

Engineer: Aries/Jesse

Size	Project Name	Rev
C	1215	1.0

Date: Monday, May 24, 2010 Sheet 70 of 97


U7001B
75 FBA_D[63..0]
FBA_D0 D22
FBA_D1 E24
FBA_D2 E22
FBA_D3 D24
FBA_D4 D26
FBA_D5 D27
FBA_D6 C27
FBA_D7 B27
FBA_D8 A21
FBA_D9 B21
FBA_D10 C21
FBA_D11 C19
FBA_D12 C18
FBA_D13 D18
FBA_D14 B18
FBA_D15 C16
FBA_D16 E21
FBA_D17 F21
FBA_D18 D20
FBA_D19 F20
FBA_D20 D17
FBA_D21 F18
FBA_D22 D16
FBA_D23 E16
FBA_D24 A22
FBA_D25 C24
FBA_D26 D21
FBA_D27 B22
FBA_D28 C22
FBA_D29 A25
FBA_D30 B25
FBA_D31 A26
FBA_D32 U24
FBA_D33 V24
FBA_D34 V23
FBA_D35 R24
FBA_D36 T23
FBA_D37 R23
FBA_D38 P24
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FBA_D40 AC24
FBA_D41 AB23
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FBA_D43 W24
FBA_D44 AA22
FBA_D45 W23
FBA_D46 W22
FBA_D47 V22
FBA_D48 AA25
FBA_D49 W27
FBA_D50 W26
FBA_D51 W25
FBA_D52 AB25
FBA_D53 AB26
FBA_D54 AD26
FBA_D55 AD27
FBA_D56 V25
FBA_D57 R25
FBA_D58 V26
FBA_D59 V27
FBA_D60 R26
FBA_D61 T25
FBA_D62 N25
FBA_D63 N26
75 FBA_DQM[7..0]
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FBA_DQM1 B19
FBA_DQM2 D19
FBA_DQM3 D23
FBA_DQM4 T24
FBA_DQM5 AA23
FBA_DQM6 AB27
FBA_DQM7 T26
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FBA_DQS_WP0 C25
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FBA_DQS_WP2 E19
FBA_DQS_WP3 A24
FBA_DQS_WP4 T22
FBA_DQS_WP5 AA24
FBA_DQS_WP6 AA26
FBA_DQS_WP7 T27
75 FBA_DQS_RN[7..0]
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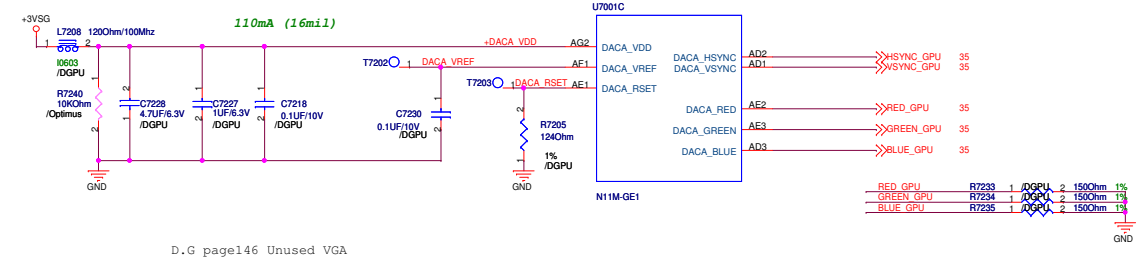
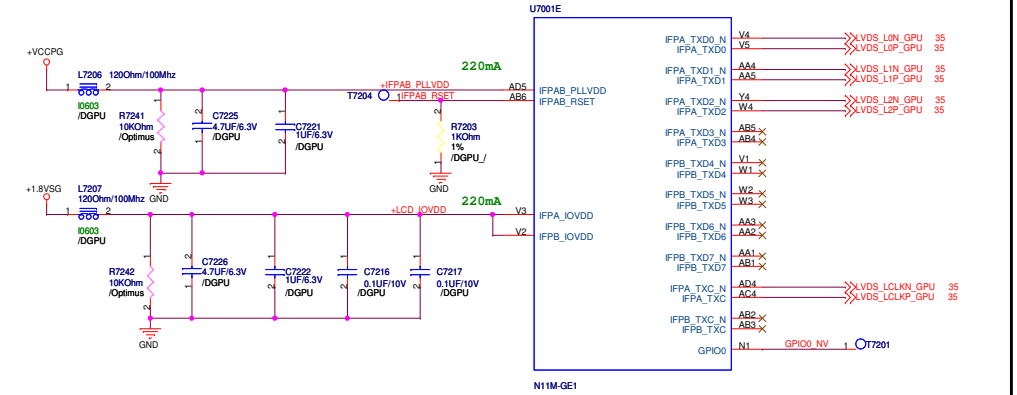
FBA_DQS_RN1 A18
FBA_DQS_RN2 E18
FBA_DQS_RN3 B24
FBA_DQS_RN4 R22
FBA_DQS_RN5 Y24
FBA_DQS_RN6 AA27
FBA_DQS_RN7 R27
+1.5VSG
R7103 1KOhm 1%
FB_VREF A16
R7104 1KOhm 1%
C7125 0.01UF/16V
GND
FBA_D0 FBA_D1 FBA_D2 FBA_D3 FBA_D4 FBA_D5 FBA_D6 FBA_D7 FBA_D8 FBA_D9 FBA_D10 FBA_D11 FBA_D12 FBA_D13 FBA_D14 FBA_D15 FBA_D16 FBA_D17 FBA_D18 FBA_D19 FBA_D20 FBA_D21 FBA_D22 FBA_D23 FBA_D24 FBA_D25 FBA_D26 FBA_D27 FBA_D28 FBA_D29 FBA_D30 FBA_D31 FBA_D32 FBA_D33 FBA_D34 FBA_D35 FBA_D36 FBA_D37 FBA_D38 FBA_D39 FBA_D40 FBA_D41 FBA_D42 FBA_D43 FBA_D44 FBA_D45 FBA_D46 FBA_D47 FBA_D48 FBA_D49 FBA_D50 FBA_D51 FBA_D52 FBA_D53 FBA_D54 FBA_D55 FBA_D56 FBA_D57 FBA_D58 FBA_D59 FBA_D60 FBA_D61 FBA_D62 FBA_D63
FBA_DQM0 FBA_DQM1 FBA_DQM2 FBA_DQM3 FBA_DQM4 FBA_DQM5 FBA_DQM6 FBA_DQM7
FBA_DQS_WP0 FBA_DQS_WP1 FBA_DQS_WP2 FBA_DQS_WP3 FBA_DQS_WP4 FBA_DQS_WP5 FBA_DQS_WP6 FBA_DQS_WP7
FBA_DQS_RN0 FBA_DQS_RN1 FBA_DQS_RN2 FBA_DQS_RN3 FBA_DQS_RN4 FBA_DQS_RN5 FBA_DQS_RN6 FBA_DQS_RN7
FB_VREF
N11M-GE1
FBVDDQ_01 A13
FBVDDQ_2 B13
FBVDDQ_3 C13
FBVDDQ_4 D13
FBVDDQ_5 D14
FBVDDQ_6 E13
FBVDDQ_7 F13
FBVDDQ_8 F14
FBVDDQ_9 F15
FBVDDQ_10 F16
FBVDDQ_11 F17
FBVDDQ_12 F19
FBVDDQ_13 F22
FBVDDQ_14 H23
FBVDDQ_15 H26
FBVDDQ_16 J15
FBVDDQ_17 J16
FBVDDQ_18 J18
FBVDDQ_19 J19
FBVDDQ_20 L19
FBVDDQ_21 L23
FBVDDQ_22 L26
FBVDDQ_23 M19
FBVDDQ_24 N22
FBVDDQ_25 U22
FBVDDQ_26 Y22
2.5A
C7117 0.1UF/10V
C7115 0.1UF/10V
C7105 0.1UF/10V
C7109 0.1UF/10V
C7113 0.22UF/10V c0402
C7103 1UF/6.3V
C7101 4.7UF/6.3V c0603
+1.5VSG
GND
C7118 0.1UF/10V
C7111 0.1UF/10V
C7108 0.1UF/10V
C7110 0.1UF/10V
C7116 0.22UF/10V c0402
C7104 1UF/6.3V
C7102 4.7UF/6.3V c0603
GND
FBA_CMD[30..0] 75
FBA_CMD0 F26
FBA_CMD1 J24
FBA_CMD2 F25
FBA_CMD3 M23
FBA_CMD4 N27
FBA_CMD5 M27
FBA_CMD6 K26
FBA_CMD7 J25
FBA_CMD8 J27
FBA_CMD9 G23
FBA_CMD10 G26
FBA_CMD11 J23
FBA_CMD12 M25
FBA_CMD13 K27
FBA_CMD14 G25
FBA_CMD15 L24
FBA_CMD16 K23
FBA_CMD17 K24
FBA_CMD18 G22
FBA_CMD19 K25
FBA_CMD20 H22
FBA_CMD21 M26
FBA_CMD22 H24
FBA_CMD23 F27
FBA_CMD24 J26
FBA_CMD25 G24
FBA_CMD26 G27
FBA_CMD27 M24
FBA_CMD28 K22
FBA_CMD29 J22
FBA_CMD30 L22
FBA_CLK0 F24
FBA_CLK0_N F23
FBA_CLK1 N24
FBA_CLK1_N N23
FBA_CLK0 75
FBA_CLK0# 75
FBA_CLK1 75
FBA_CLK1# 75
+1.5VSG
M22 FBA_DEBUG R7106 10KOhm
FBA_DEBUG(CAS2_for_GDDR3 designs)
+1.5VSG
FB_CAL_PD_VDDQ B15 FB_CAL_PD_VDDQ R7112 40.2Ohm 1%
FB_CAL_PU_GND A15 FB_CAL_PU_GND R7115 40.2Ohm 1%
FB_CAL_TERM_GND B16 FB_CAL_TERM_GND R7116 60.4Ohm 1%
GND
+VCCPG
FB_PLLAVDD_2 R19
FB_DLLAVDD T19
FB_PLLAVDD_3 AC19
+FB_PLLAVDD
20mil
L7101 120Ohm/100Mhz
C7112 0.1UF/10V
C7124 1UF/6.3V
C7122 4.7UF/6.3V I0603
c0603
GND
<Variant Name>
Title : VGA_nVIDIA_N11M-GE2_FB
ASUSTeK COMPUTER INC
Engineer: Aries/Jesse
Size Custom
Project Name 1215
Rev 1.0
Date: Monday, May 24, 2010
Sheet 71 of 97

VGA



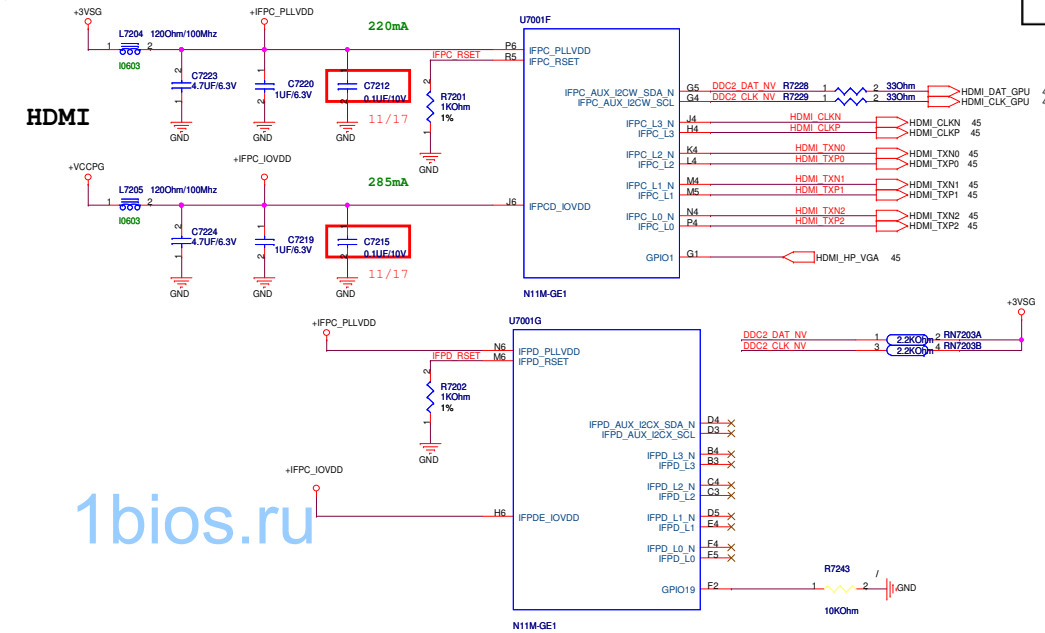
D.G page146 Unused VGA
DAC_VDD tie to GND via a 10Kohm
Other pins can be N.C

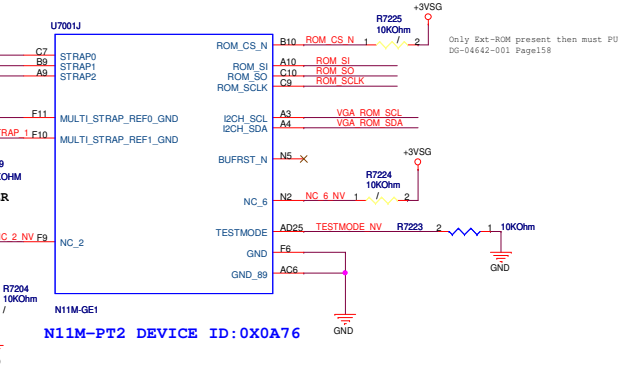
LVDS



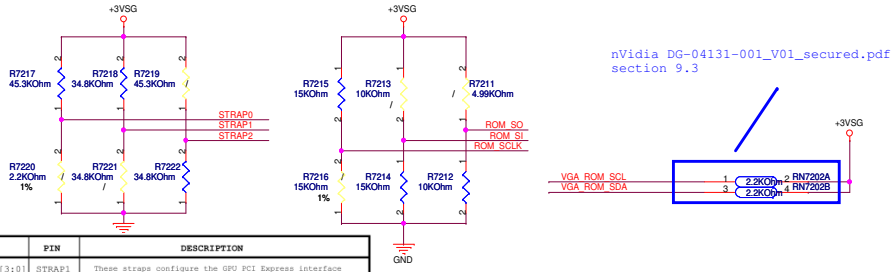
D.G page146 Unused IFPA/B
IFPAB_PLVDD/IFPA_B_IOVDD tie to GND via a 10Kohm
Other pins can be N.C

HDMI





N11M-PT2 DEVICE ID:0X0A76



STRAPS	PIN	DESCRIPTION
3GIO_PADCFG[3:0]	STRAP1	These straps configure the GPU PCI Express interface 0000 - Reserved 0010 - Notebook(Mothbook Default) 0011 - Reserved 0100 - Reserved 0101...1110 - Reserved 1111 - Reserved

PUN-04741 setting 1110

STRAPS	PIN	DESCRIPTION
USER[3:0]	STRAP0	USER[3:0] straps can be used if on-board straps are needed to identify the panel for notebook design User[3:0] Type Resolution Sync Note 0000 XGA 1024X768 -/- 0001 XGA 1024X768 +/+ 0010 SXGA 1280X1024 -/- 0011 SXGA+ 1400X1050 -/- 0100 UXGA 1600X1200 +/+ 0101 QXGA 2048X1536 +/+ Reduced Blanking 0110 SXGA+ 1400X1050 -/- 0111 SVGA 800X600 +/+ 1000-1100 - - Customer defined(Default) 1111 - - EDID is used

Multilevel Strapping Options

Physical Strapping Pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	PEX_PLL_EN_THRM	
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	VDD33	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]

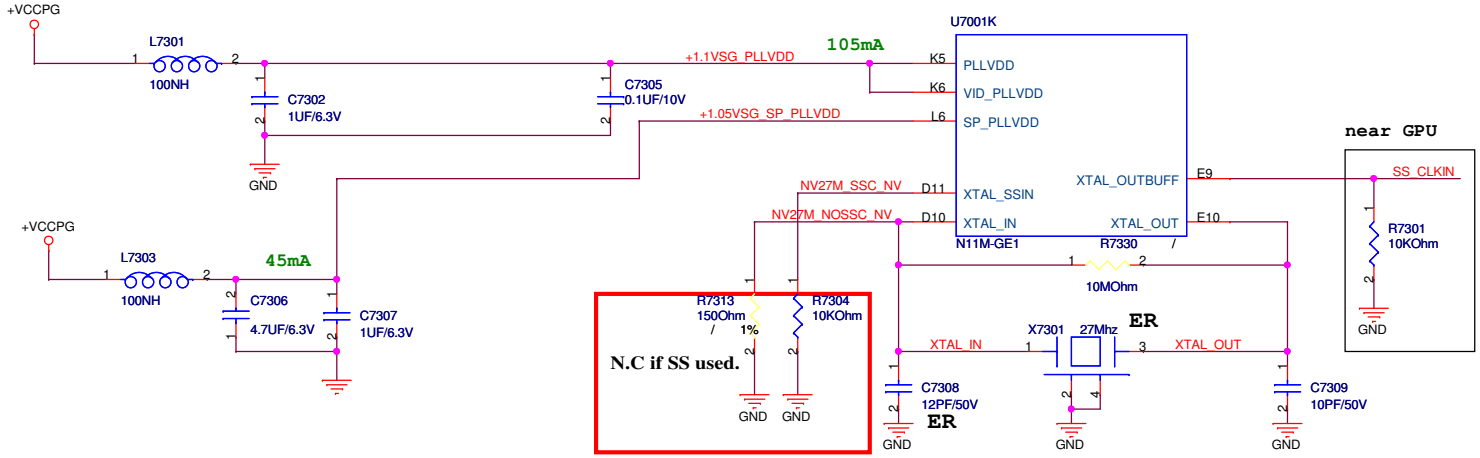
Logical Strap Bit Mapping

Resistor Value	Pull-Up to VDD	Pull-Down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

STRAPS	PIN	DESCRIPTION
XCLK	ROM_SO	Control the output frequency of the internal PCI-Express Clock.This must be strapped to logic"0" for correct functionality 0= 277MHz(Default) 1= Reserved
FB_0_BAR_SIZE	ROM_SO	Select the system frame buffer aperture size used by the GPU 0= 256MB(Default) 1= Reserved
SMB_ALT_ADDR	ROM_SO	Configure the I2C address of a GPU 0= 0x9E(Default) 1= 0x9C(Multi-GPU usage)
VGA_DEVICE	ROM_SO	Used to identify the device type of the GPU within the PCI configuration space 0= 3D Device(Class Code 302h) 1= VGA Device(Default-Class Code 302h)
PCI_DEVID[4]	ROM_SCLK	nVIDIA GPU PCI Device IDs straps(Refer to PUN or Datasheet)
SUB_VENDOR	ROM_SCLK	Determines if the VBIOS is integrated with SBIOS(BIOS not present) or if it is in a separate video ROM(BIOS present) 0= No Video BIOS ROM 1= BIOS ROM is present(Default)
SLOT_CLK_CFG	ROM_SCLK	Pull this strap high if the GPU and MCH share a common PCI Express reference clock, for example from the same clock generator chip 0= GPU & MCH dot not share 1= GPU & MCH share(Default)
PEX_PLL_EN_THRM	ROM_SCLK	To set the PCI Express PLL termination enable 0= Disable(Default) 1= Enable
PCI_DEVID[3:0]	STRAP2	nVIDIA GPU PCI Device IDs are typically specified in the 32-bit register PCI_NV_0[31:0]. Bits[31:5] are fixed in silicon;bits[4:0] can be changed using the PCI_DEVID straps.Refer to the relevant data sheets & PUN for the PCI Device ID informaton.

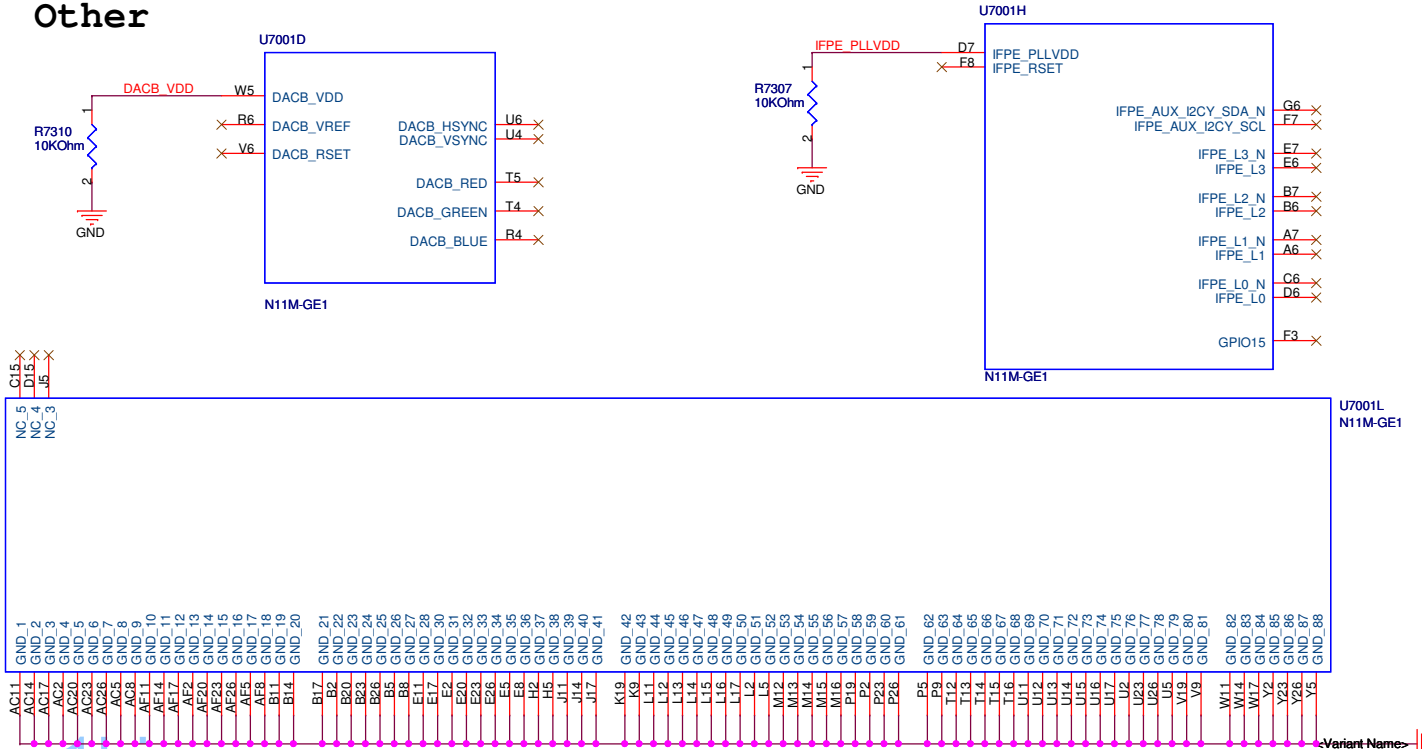
STRAPS	PIN	DESCRIPTION
RAMCFG[3:0]	ROM_SI	MEMORY TYPE,MAKE AND SIZE INFO 0010 - DDR3 64Mx16 HYNIX/H5TQ1G63BFR-12C 0011 - DDR3 64Mx16 Samsung/K4W1G1646E-HC12 TBD

Xtal



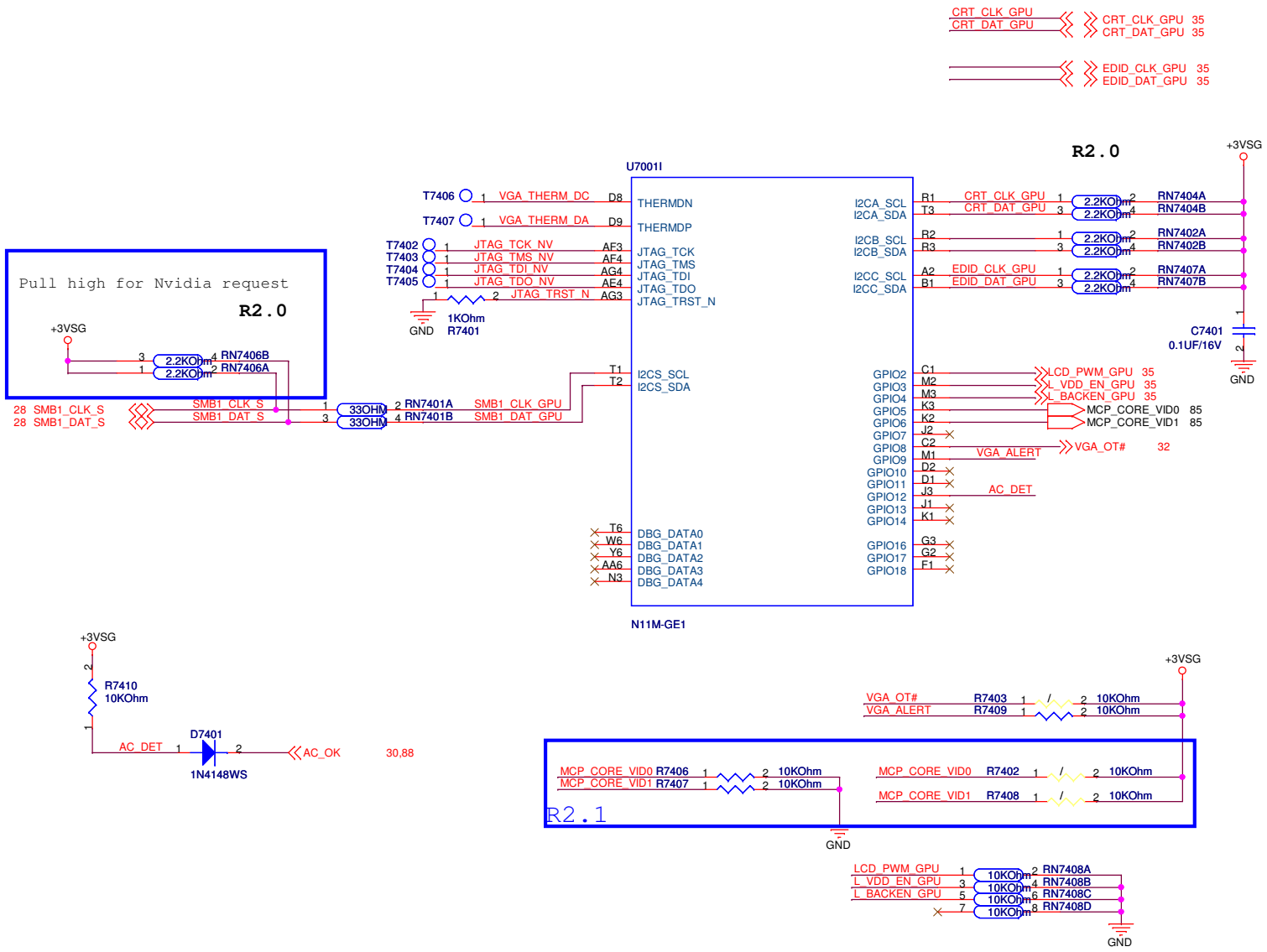
ER:加高没有symbol,先用EPSON的

Other



<Variant Name>

ASUSTeK COMPUTER INC	Title : VGA_nVIDIA_N11M-GE2_XTAL	
	Engineer: Aries/Jesse	
Size: Custom	Project Name: 1215	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 73 of 97	



GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	NVGEM
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVVDD VID 0
6	OUT	HIGH	NVVDD VID 1
7	OUT	HIGH	FBVDD VID 0
8	IN/OUT	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	HIGH	FBVREF SELECT
11	OUT	HIGH	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL 0
14	OUT	HIGH	PS CONTROL 1

MCP_CORE_VID0	MCP_CORE_VID1	+0.89VS
L	L	0.848V
H	L	0.896V
H	H	0.945V
L	H	0.896V

<Variant Name>

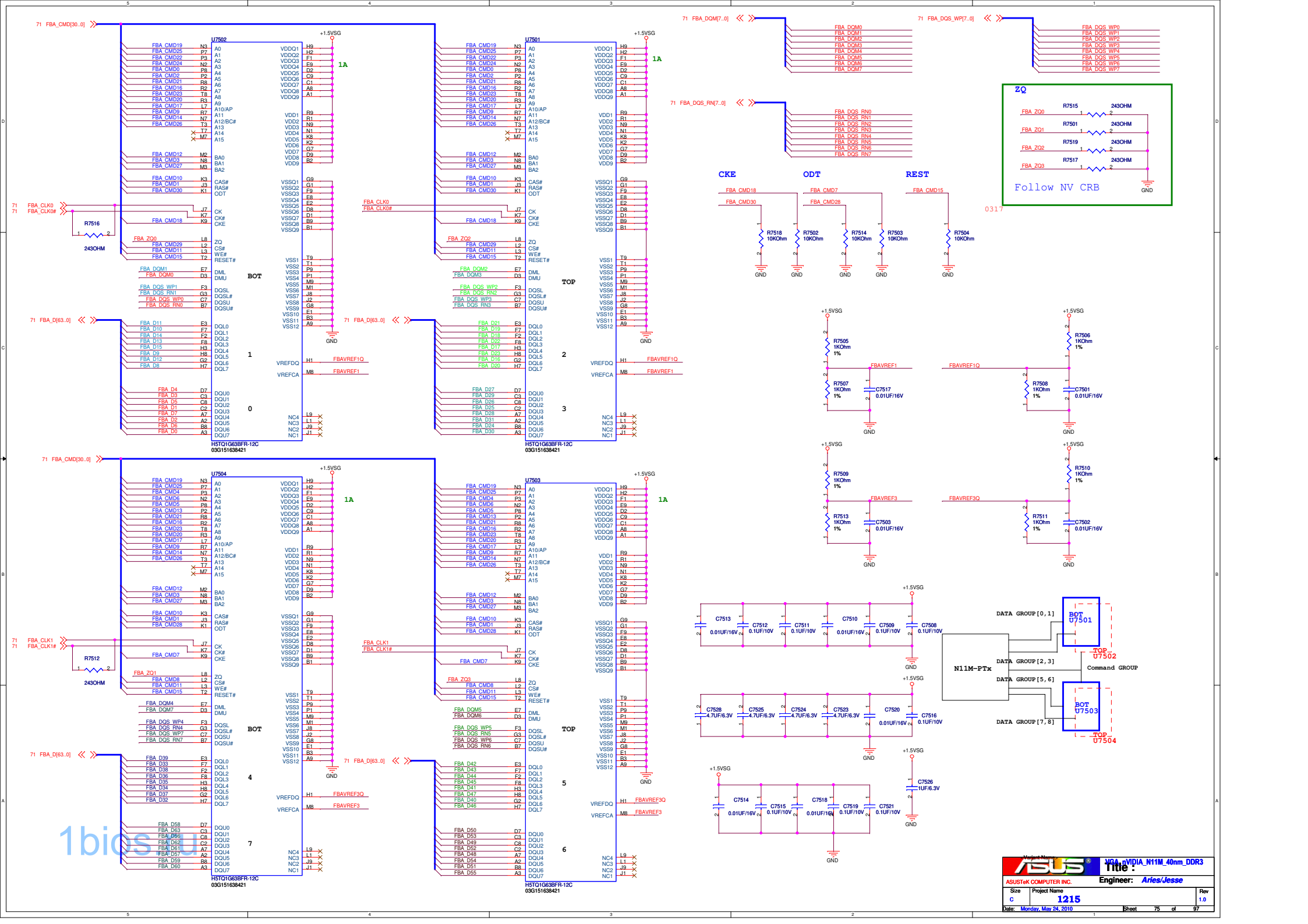
Title : VGA_nVIDIA_N11M-GE2_GPIO

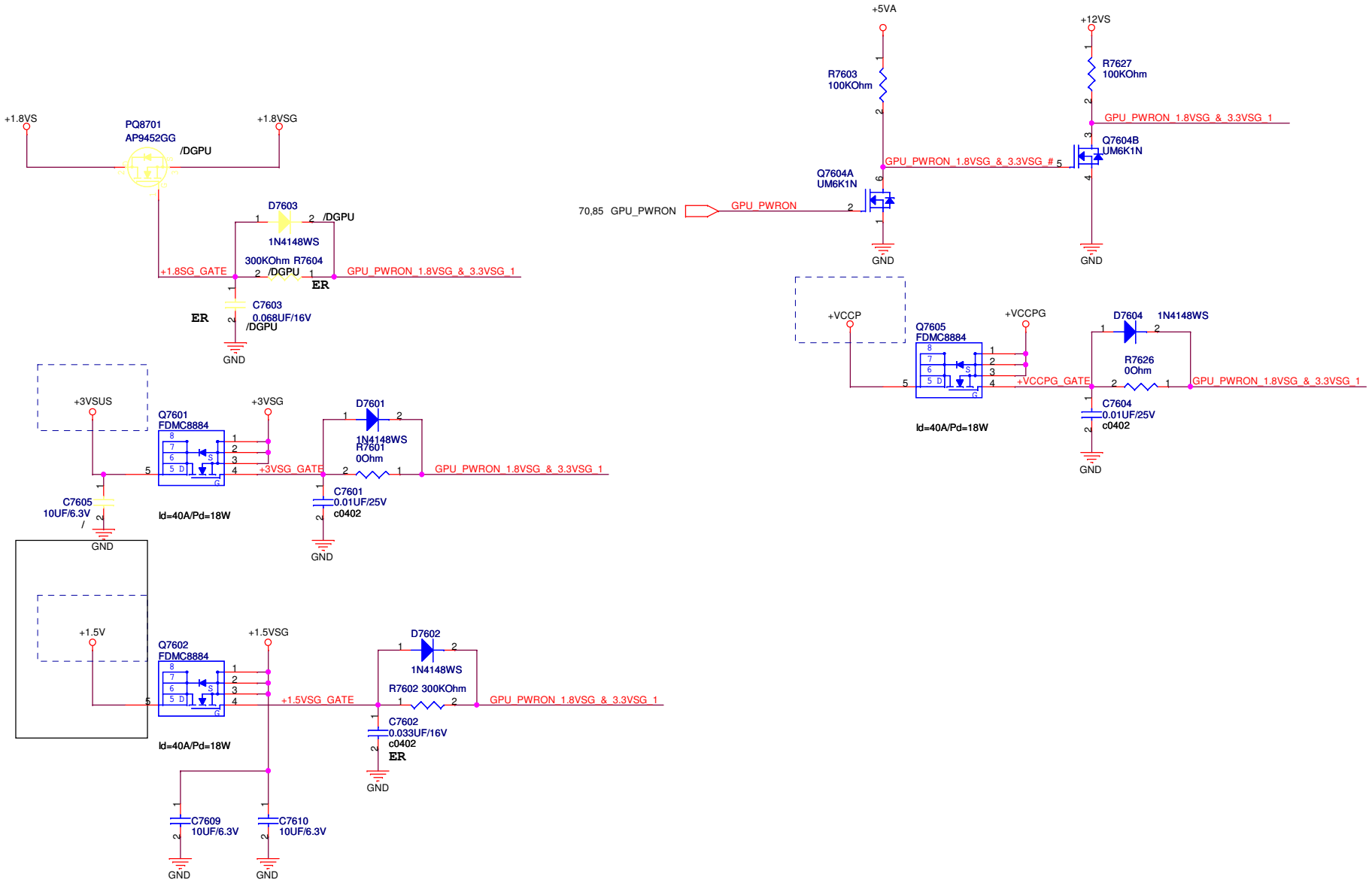
ASUSTeK COMPUTER INC

Engineer: Aries/Jesse

Size	Project Name	Rev
Custom	1215	1.0

Date: Monday, May 24, 2010 Sheet 74 of 97


U7502
U7501
U7504
U7503
H5TQ1G63BFR-12C
03G151638421
BOT
TOP
1A
+1.5VSG
GND
R7516
R7512
243OHM
CKE
ODT
REST
ZQ
Follow NV CRB
R7515 243OHM
R7501 243OHM
R7519 243OHM
R7517 243OHM
R7518 10KOhm
R7502 10KOhm
R7514 10KOhm
R7503 10KOhm
R7504 10KOhm
R7505 1KOhm 1%
R7506 1KOhm 1%
R7507 1KOhm 1%
R7508 1KOhm 1%
R7509 1KOhm 1%
R7510 1KOhm 1%
R7513 1KOhm 1%
R7511 1KOhm 1%
C7517 0.01UF/16V
C7501 0.01UF/16V
C7503 0.01UF/16V
C7502 0.01UF/16V
C7513 0.01UF/16V
C7512 0.1UF/10V
C7511 0.1UF/10V
C7510 0.01UF/16V
C7509 0.1UF/10V
C7508 0.1UF/10V
C7528 4.7UF/6.3V
C7525 4.7UF/6.3V
C7524 4.7UF/6.3V
C7523 4.7UF/6.3V
C7520 0.01UF/16V
C7516 0.1UF/10V
C7514 0.01UF/16V
C7515 0.1UF/10V
C7518 0.01UF/16V
C7519 0.1UF/10V
C7521 0.1UF/10V
C7526 1UF/6.3V
N11M-PTx
DATA GROUP[0,1]
DATA GROUP[2,3]
DATA GROUP[5,6]
DATA GROUP[7,8]
Command GROUP
BOT U7501
TOP U7502
BOT U7503
TOP U7504
FBAVREF1
FBAVREF1Q
FBAVREF3
FBAVREF3Q
ASUSTeK COMPUTER INC.
Engineer: Aries/Jesse
Title : VGA_nVIDIA_N11M_40nm_DDR3
Size C
Project Name 1215
Rev 1.0
Date: Monday, May 24, 2010
Sheet 75 of 97



<Variant Name>

Title :	VGA-Power
ASUSTeK COMPUTER INC	Engineer: Aries/Jesse
Size: B	Project Name: 1215
Rev: 2.1	
Date: Monday, May 24, 2010	Sheet 76 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

Size	Project Name	Rev
A	UL20A	2.1

Date: Monday, May 24, 2010 Sheet 77 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

Size	Project Name	Rev
A	UL20A	2.1

Date: Monday, May 24, 2010 Sheet 78 of 97

<Variant Name>

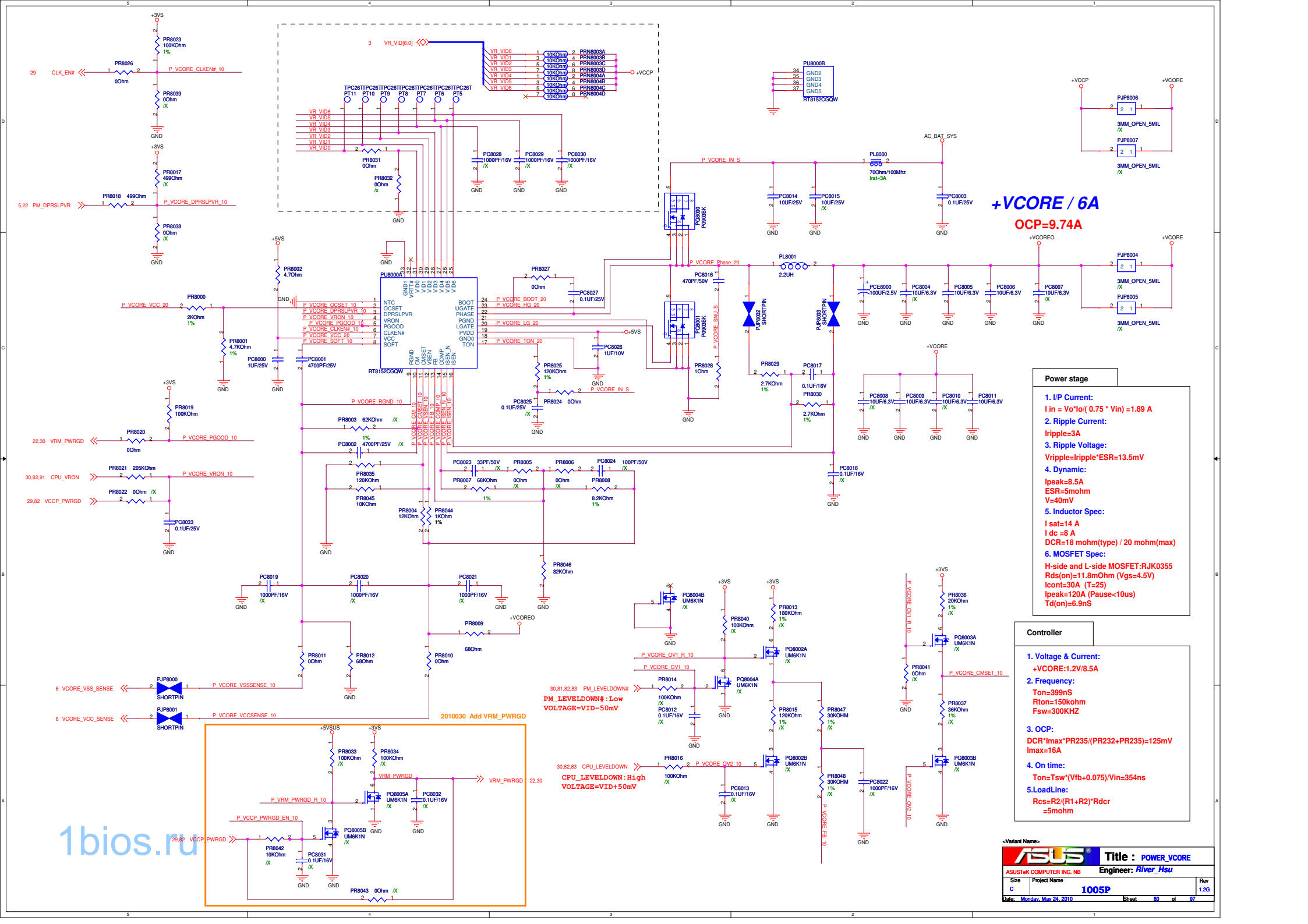
Title :

ASUSTeK COMPUTER INC

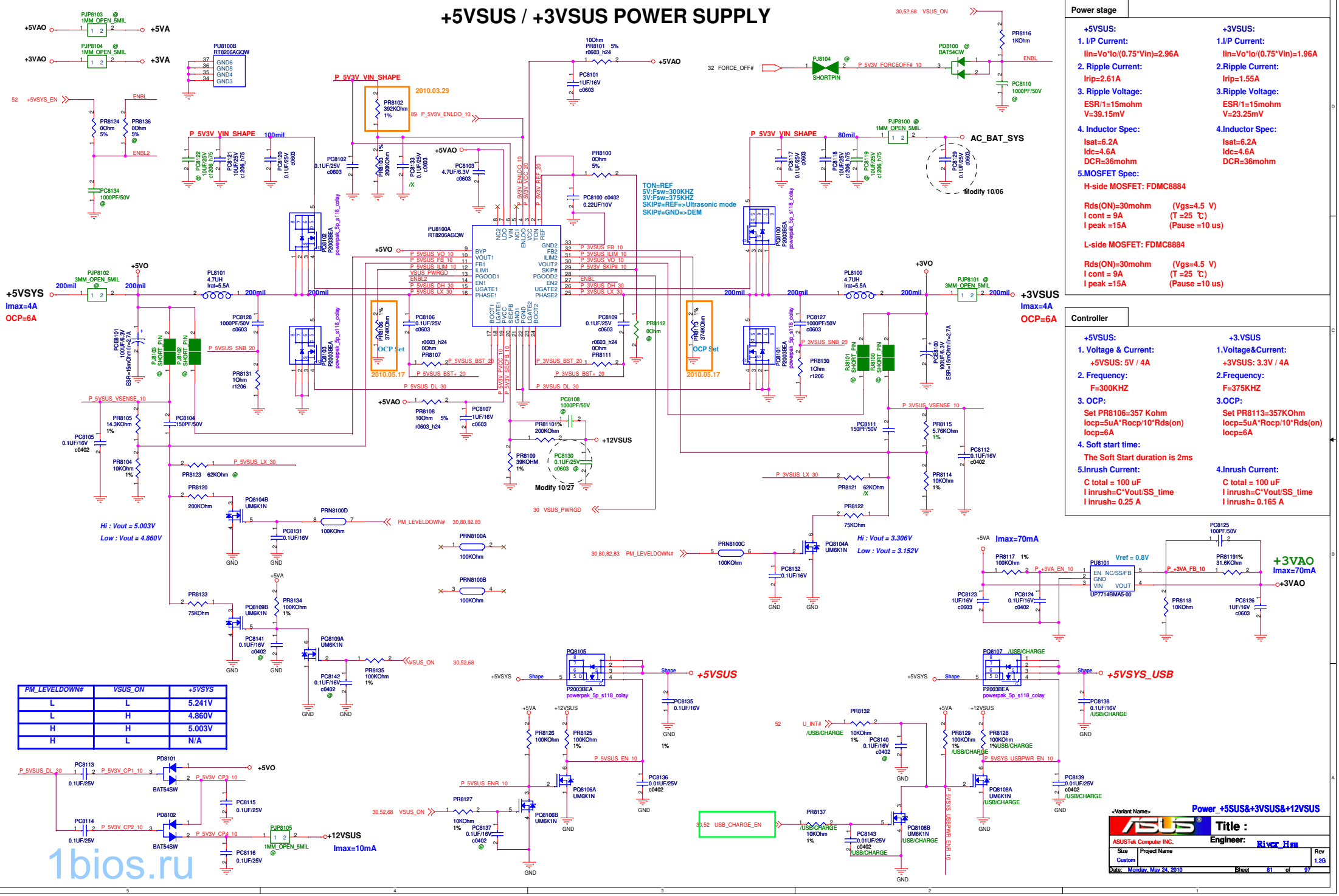
Engineer: Jerry Yu

Size	Project Name	Rev
A	UL20A	2.1

Date: Monday, May 24, 2010 Sheet 79 of 97


+VCORE / 6A
OCP=9.74A
Power stage
1. I/P Current:
I in = Vo*Io/(0.75 * Vin) =1.89 A
2. Ripple Current:
Iripple=3A
3. Ripple Voltage:
Vripple=Iripple*ESR=13.5mV
4. Dynamic:
Ipeak=8.5A
ESR=5mohm
V=40mV
5. Inductor Spec:
I sat=14 A
I dc =8 A
DCR=18 mohm(type) / 20 mohm(max)
6. MOSFET Spec:
H-side and L-side MOSFET:RJK0355
Rds(on)=11.8mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)
Td(on)=6.9nS
Controller
1. Voltage & Current:
+VCORE:1.2V/8.5A
2. Frequency:
Ton=399nS
Rton=150kohm
Fsw=300KHZ
3. OCP:
DCR*Imax*PR235/(PR232+PR235)=125mV
Imax=16A
4. On time:
Ton=Tsw*(Vfb+0.075)/Vin=354ns
5.LoadLine:
Rcs=R2/(R1+R2)*Rdcr
=5mohm
PM_LEVELDOWN#:Low
VOLTAGE=VID-50mV
CPU_LEVELDOWN:High
VOLTAGE=VID+50mV
2010030 Add VRM_PWRGD
RT8152CGQW
Title : POWER_VCORE
ASUSTeK COMPUTER INC. NB
Engineer: River_Hsu
Project Name
1005P
Rev
1.2G
Monday, May 24, 2010
Sheet 80 of 97
1bios.ru

+5VSUS / +3VSUS POWER SUPPLY



PM_LEVELDOWN#	VSUS_ON	+5VSYS
L	L	5.241V
L	H	4.860V
H	H	5.003V
H	L	N/A

Power stage

+5VSUS:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.96A
2. Ripple Current:
   Irip=2.61A
3. Ripple Voltage:
   ESR/1=15mohm
   V=39.15mV
4. Inductor Spec:
   Isat=6.2A
   Idc=4.6A
   DCR=36mohm
5. MOSFET Spec:
   H-side MOSFET: FDMC8884

   Rds(ON)=30mohm (Vgs=4.5 V)
   I cont = 9A (T =25 ℃)
   I peak =15A (Pause =10 us)

   L-side MOSFET: FDMC8884

   Rds(ON)=30mohm (Vgs=4.5 V)
   I cont = 9A (T =25 ℃)
   I peak =15A (Pause =10 us)

+3VSUS:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.96A
2. Ripple Current:
   Irip=1.55A
3. Ripple Voltage:
   ESR/1=15mohm
   V=23.25mV
4. Inductor Spec:
   Isat=6.2A
   Idc=4.6A
   DCR=36mohm

Controller

+5VSUS:

1. Voltage & Current:
   +5VSUS: 5V / 4A
2. Frequency:
   F=300KHZ
3. OCP:
   Set PR8106=357 Kohm
   Iocp=5uA*Rocp/10*Rds(on)
   Iocp=6A
4. Soft start time:
   The Soft Start duration is 2ms
5. Inrush Current:
   C total = 100 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.25 A

+3.VSUS

1. Voltage&Current:
   +3VSUS: 3.3V / 4A
2. Frequency:
   F=375KHZ
3. OCP:
   Set PR8113=357KOhm
   Iocp=5uA*Rocp/10*Rds(on)
   Iocp=6A
4. Inrush Current:
   C total = 100 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.165 A

<variant_name> Power_+5SUS&+3VSUS&+12VSUS

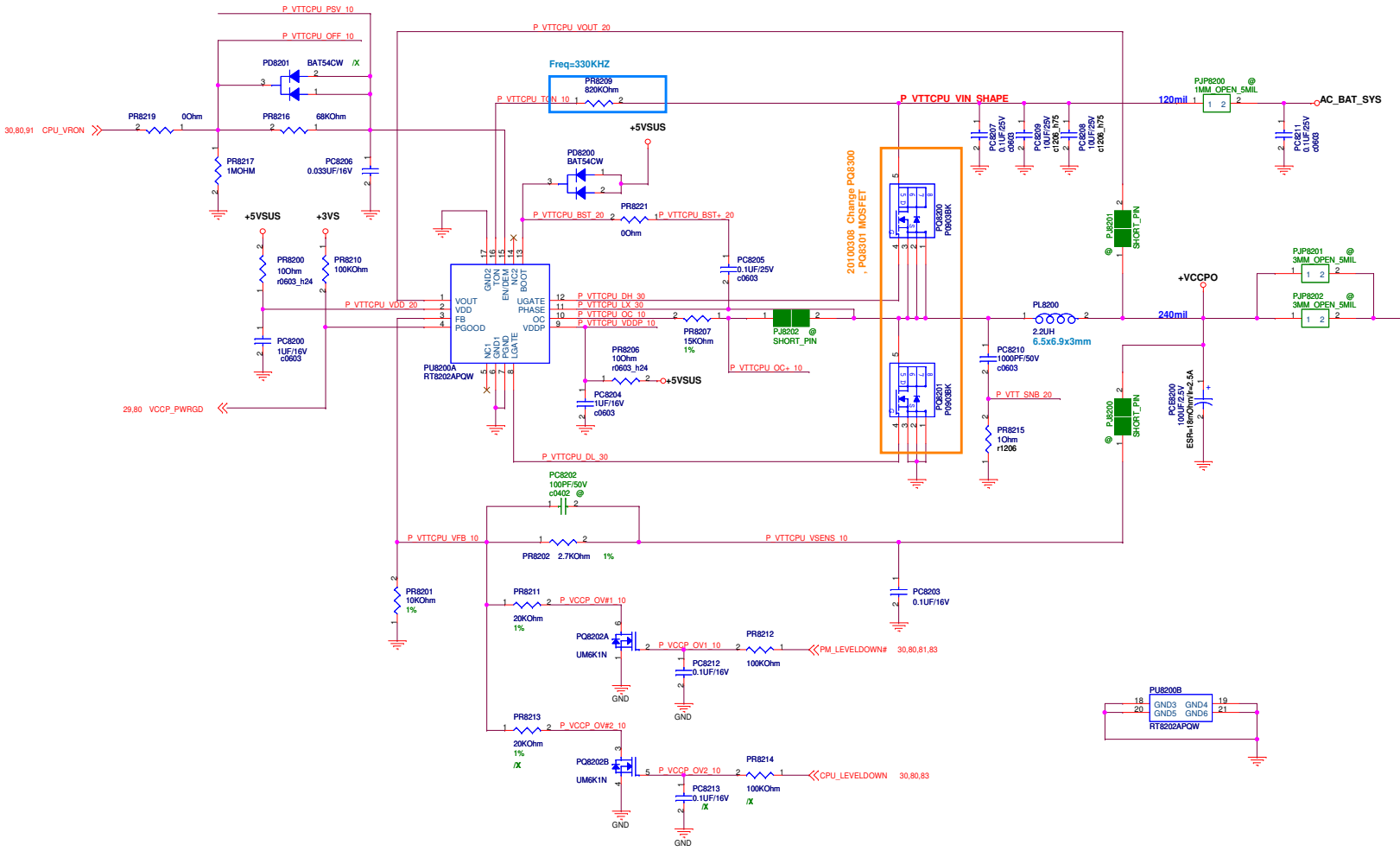
Title :

ASUSTek Computer INC. Engineer: River Hu

Size	Project Name	Rev
Custom		1.2G

Date: Monday, May 24, 2010 Sheet 81 of 97

+VCCP



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.953V	Power Saving
H	L	H	1.054V	Normal
H	H	L	N/A	Performance
L	H	L	N/A	N/A

Controller

+VTT_CPU:

1. Voltage & Current:
   +VTT_CPU: 1.05V / 15A
2. Frequency:
   F=330KHZ
3. OCP:
   Set PR8207=4.99 Kohm
   Iocp=Rocp*20uA/Rds(on)
   Iocp=26A
4. Soft start time:
   The SS duration is 1.35ms
5. Inrush Current:
   C total = 440 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.342 A

Power stage

+VTT_CPU:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.33A
2. Ripple Current:
   Irip=5.36A
3. Ripple Voltage:
   ESR/2=7.5mohm
   Vripple=40.26mV
4. Inductor Spec:
   Isat=40A
   Idc=25A
   DCR=1.6mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

   L-side MOSFET: RJK0353DPA

   Rds(ON)=7.6mohm (Vgs=4.5 V)
   I cont = 35A (T =25 ℃)
   I peak =140 A (Pause =10 us)

<Variant Name>

ASUSTek Computer INC.

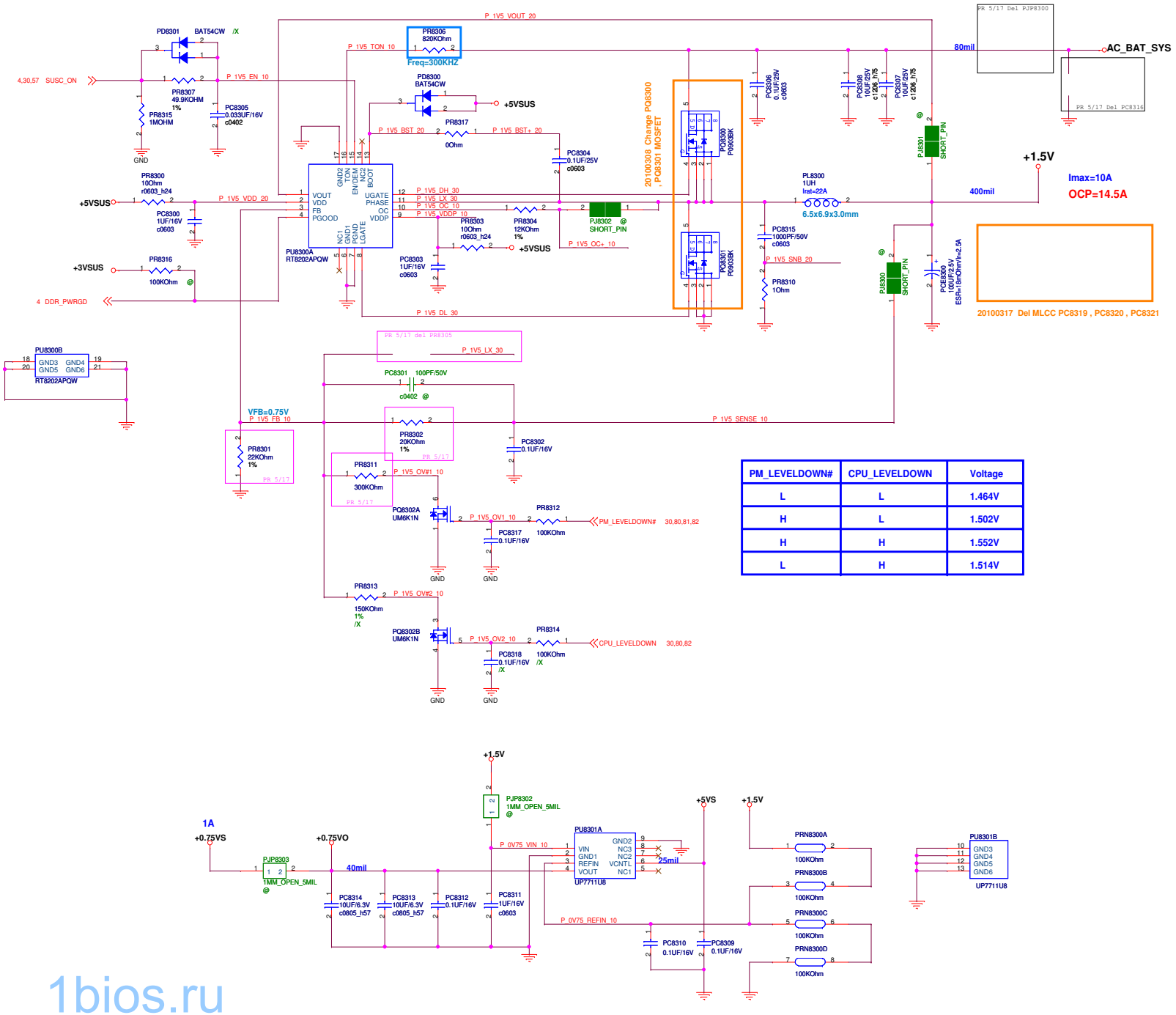
Title : +VCCP

Engineer: River_Hsu

Size	Project Name	Rev
C	1005P	1.2G

Date: Monday, May 24, 2010 Sheet 82 of 97

+1.8V & +0.9VS POWER SUPPLY



PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage
L	L	1.464V
H	L	1.502V
H	H	1.552V
L	H	1.514V

Power stage

DDR III:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.22A
2. Ripple Current:
   Irip=4.62A
3. Ripple Voltage:
   ESR/1=15mohm
   V=69.3mV
4. Inductor Spec:
   Isat=12.7A
   Idc=9.5A
   DCR=8.5mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

   L-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

Controller

DDR III:

1. Voltage & Current:
   +1.5V: 1.5V / 10A
2. Frequency:
   F=300KHZ
3. OCP:
   Set R8302=12 Kohm
   Iocp=Rocp*20uA/Rds(on)
   Iocp=14.3A
4. Soft start time:
   The Soft Start duration is 1.35ms
5. Inrush Current:
   C total = 220 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.244 A

1. Voltage & Current:
   +0.75V: 0.75V / 1A

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : +1.5VS&+1.2VS

Engineer: River_Hsu

Size	Project Name	Rev
Custom	1005HT	1.2G

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<Variant Name>

Title : +1.8V & VTTDDR

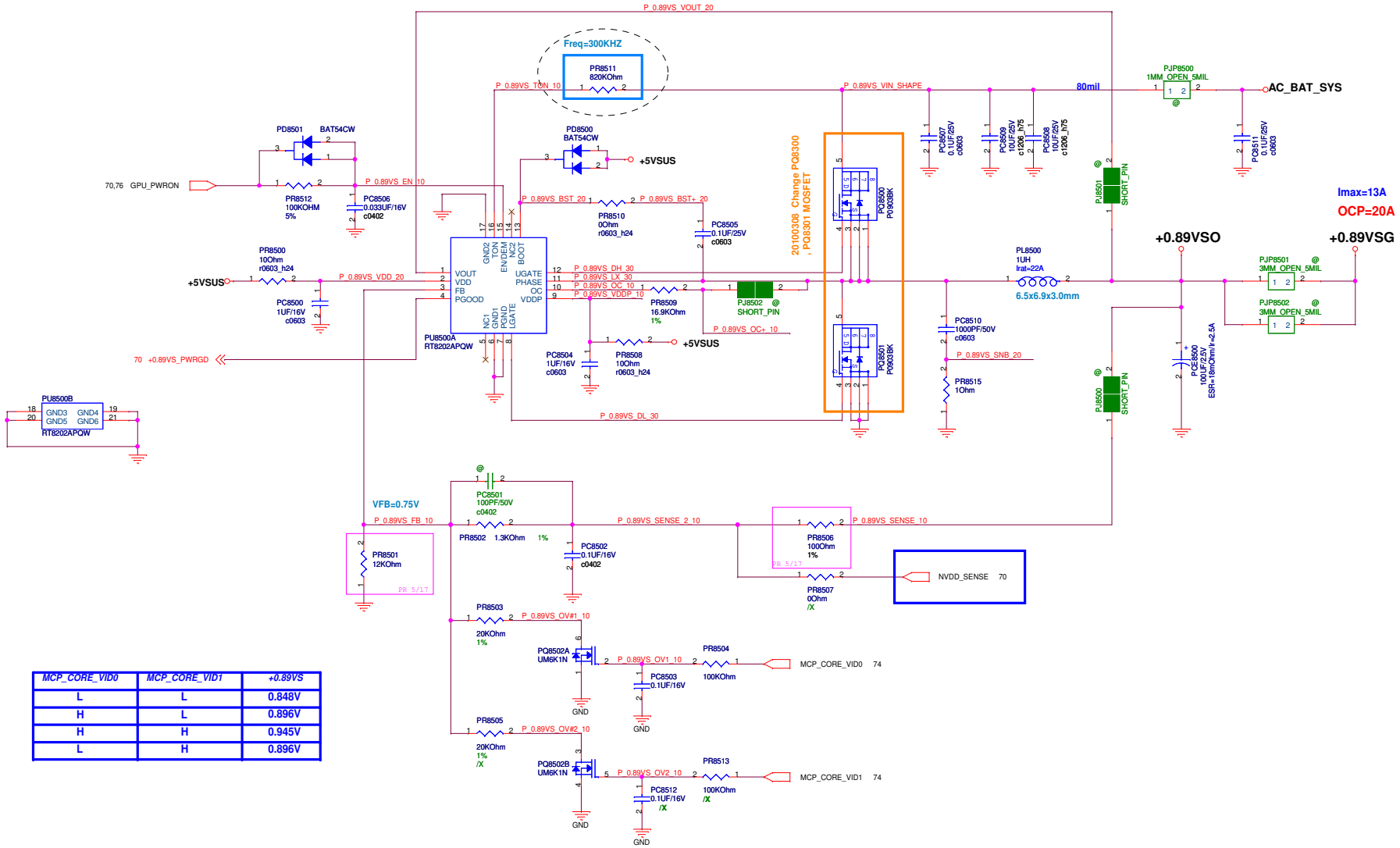
ASUSTek Computer INC.

Engineer: River_Hsu

Size	Project Name	Rev
C	1005P	1.2G

Date: Monday, May 24, 2010 Sheet 84 of 97

GPU NVDD POWER SUPPLY



MCP_CORE_VID0	MCP_CORE_VID1	+0.89VS
L	L	0.848V
H	L	0.896V
H	H	0.945V
L	H	0.896V

Power stage

NVDD:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=2.11A

2. Ripple Current:

Irip=7.59A

3. Ripple Voltage:

ESR/2=7.5mohm
V=56.925mV

4. Inductor Spec:

Isat=26A
Idc=17.5A
DCR=4.2mohm

5.MOSFET Spec:

H-side MOSFET: RJK0355DPA

Rds(ON)=16.5mohm (Vgs=4.5 V)
I cont = 30A (T =25 ℃)
I peak =120 A (Pause =10 us)

L-side MOSFET: RJK0353DPA

Rds(ON)=7.6mohm (Vgs=4.5 V)
I cont = 35A (T =25 ℃)
I peak =140 A (Pause =10 us)

Controller

NVDD:

1. Voltage & Current:

+NVDD: 0.95V / 15A

2. Frequency:

F=253KHZ

3. OCP:

Set R8504=7.5 Kohm
Iocp=Rocp*20uA/Rds(on)
Iocp=20A

4. Soft start time:

The Soft Start duration is 1.35ms

5.Inrush Current:

C total = 440 uF
I inrush=C*Vout/SS_time
I inrush= 0.310 A

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : POWER_I/O_NVDD	
	Engineer: Matt_Wang	
Size: Custom	Project Name: Design_IP	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 85 of 97	

<Variant Name>

Title : POWER_+VGFX_CORE

<OrgName>

Engineer: Mang_Wang

Size	Project Name	Rev
Custom	Design_IP	1.0

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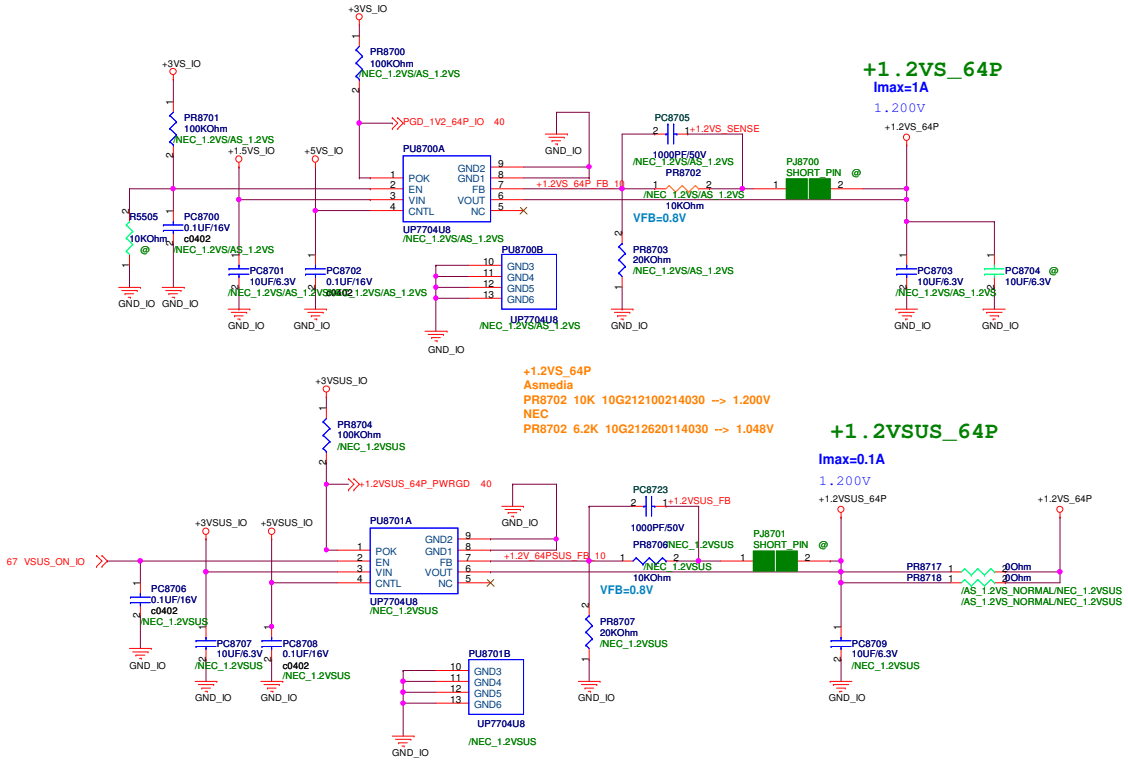

Dual_layout BOM_table	OPTIONAL CHOICE	Voltage(NEC=1.05V;ASM=1.2V)
NEC (Normal)	/NEC_1.2VS/AS_1.2VS	NEC PR8702 6.2K 10G212620114030 --> 1.048V
NEC(SUS)	/NEC_1.2VSUS	NEC PR8706 6.2K 10G212620114030 --> 1.048V
ASM1042(Normal)	/NEC_1.2VS/AS_1.2VS /AS_1.2VS_ALL NORMAL	Asmedia PR8702 10K 10G212100214030 --> 1.200V
ASM1042(Normal +SUS)	/NEC_1.2VS/AS_1.2VS /NEC_1.2VSUS	Asmedia PR8702 10K 10G212100214030 --> 1.200V Asmedia PR8706 10K 10G212100214030 --> 1.200V

Dual_layout BOM_table	BOM(USB interface)	BOM(PCIE interface)	BOM(XTL interface)	BOM(SPI interface)
ASM only (USB3.0) (USB2.0)	C4045, C4046, C4026, C4027, C4059, C4061, C4062, C4063, C4064, C4065, C4066, C4067, RN4012A, RN4012B	R4038, R4039, R4040, R4041, C4042, C4043	X4002(20MHZ, 07G010012000), @C4036,C4037(22pF,11G232022004030), C4051, R4032, @C4052	R4053, R4054, R4055, R4056, R4028/ R4029 (4.7K, 10G212472004030), C4003, U4007
NEC only (USB3.0) (USB2.0)	C1328, C1329, C1331, C1332, C1333, C1334, C1335, C1336, C1337, C1338, C1339, C1340, RN4012A, RN4012B	R1318, R1319, R1320, R1321, C1325, C1326	X4002(24MHZ,11G232027004070), C4036,C4037(12pF,11G232012004320), @C4051, R1317, @R1315, @R1316	R1324, R1325, R1326, R1327, R4028(8.2K, 10G212822004030), R4029(39.2K, 10G212392214031), C4003, U4007
PCH only (USB2.0)	RN4013A, RN4013B			
ASM+PCH (USB3.0) (USB2.0)	C4045, C4046, C4026, C4027, C4059, C4061, C4062, C4063, C4064, C4065, C4066, C4067, RN4012A, RN4012B, RN4013A, RN4013B	R4038, R4039, R4040, R4041, C4042, C4043		
NEC+PCH (USB3.0) (USB2.0)	C1328, C1329, C1331, C1332, C1333, C1334, C1335, C1336, C1337, C1338, C1339, C1340, RN4012A, RN4012B, RN4013A, RN4013B	R1318, R1319, R1320, R1321, C1325, C1326		

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : N/A

Engineer: Aaron_Lin

Size	Project Name	Rev
Custom	UL20A	1.0

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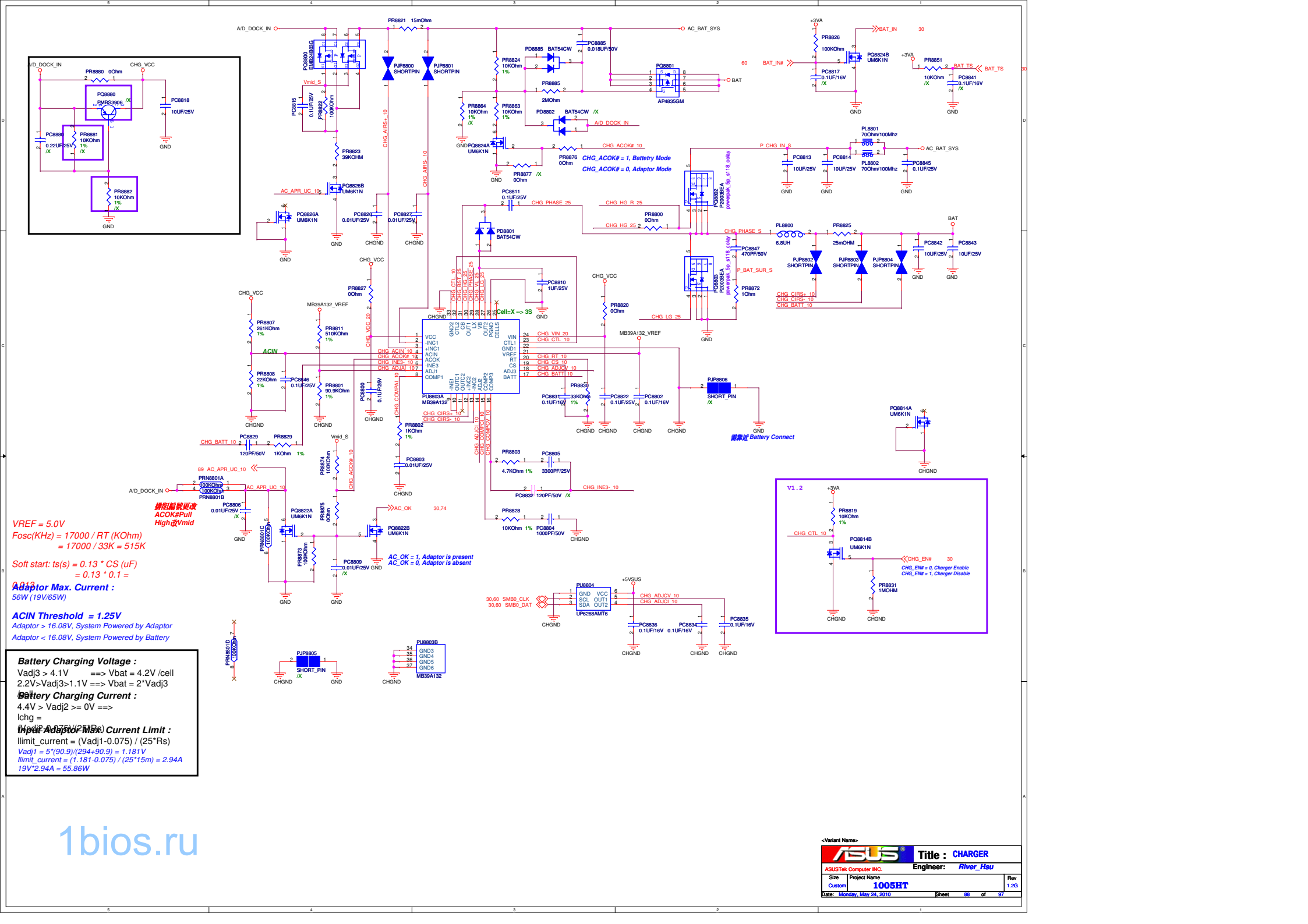
VREF = 5.0V
Fosc(KHz) = 17000 / RT (KOhm)
= 17000 / 33K = 515K
Soft start: ts(s) = 0.13 * CS (uF)
= 0.13 * 0.1 =
0.013
Adaptor Max. Current :
56W (19V/65W)
ACIN Threshold = 1.25V
Adaptor > 16.08V, System Powered by Adaptor
Adaptor < 16.08V, System Powered by Battery
Battery Charging Voltage :
Vadj3 > 4.1V ==> Vbat = 4.2V /cell
2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3
Battery Charging Current :
4.4V > Vadj2 >= 0V ==>
Ichg =
(Vadj2-0.075V/25Rs)
Input Adaptor Max. Current Limit :
Ilimit_current = (Vadj1-0.075) / (25*Rs)
Vadj1 = 5*(90.9)/(294+90.9) = 1.181V
Ilimit_current = (1.181-0.075) / (25*15m) = 2.94A
19V*2.94A = 55.86W
CHG_ACOK# = 1, Battery Mode
CHG_ACOK# = 0, Adaptor Mode
AC_OK = 1, Adaptor is present
AC_OK = 0, Adaptor is absent
Cell=X --> 3S
Title : CHARGER
Engineer: River_Hsu
ASUSTek Computer INC.
Project Name 1005HT
Rev 1.2G
Date: Monday, May 24, 2010
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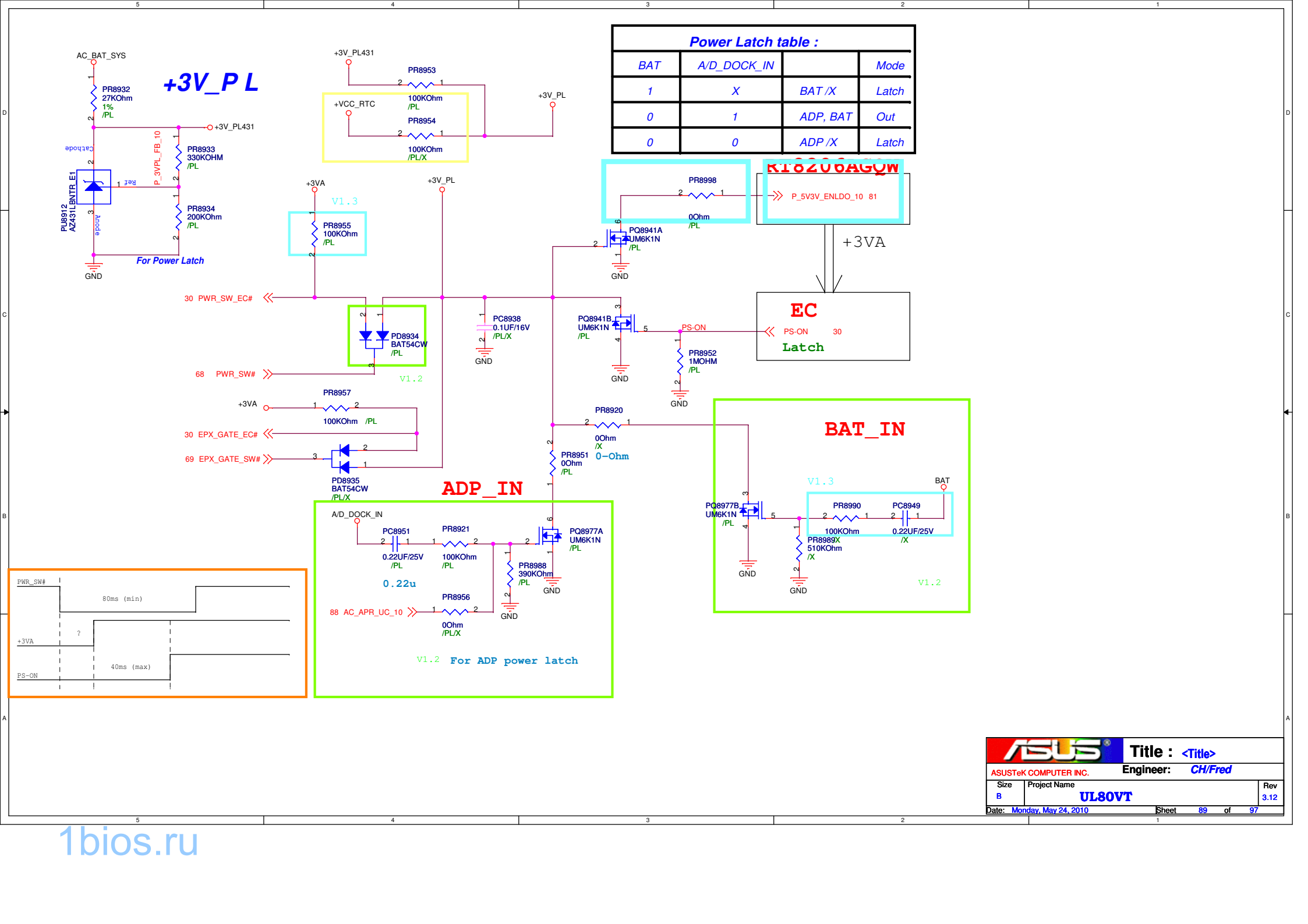
Power Latch table :
BAT | A/D_DOCK_IN | | Mode
1 | X | BAT /X | Latch
0 | 1 | ADP, BAT | Out
0 | 0 | ADP /X | Latch
+3V_P L
AC_BAT_SYS
PR8932 27KOhm 1% /PL
+3V_PL431
PR8933 330KOHM /PL
PR8934 200KOhm /PL
PU8912 AZ431LBNTR_E1
P_3VPL_FB_10
For Power Latch
GND
+3V_PL431
PR8953 100KOhm /PL
+VCC_RTC
PR8954 100KOhm /PL/X
+3V_PL
+3VA
V1.3
PR8955 100KOhm /PL
PR8998 0Ohm /PL
PQ8941A UM6K1N /PL
P_5V3V_ENLDO_10 81
+3VA
EC
PS-ON 30
Latch
30 PWR_SW_EC#
PD8934 BAT54CW /PL
PC8938 0.1UF/16V /PL/X
PQ8941B UM6K1N /PL
PS-ON
PR8952 1MOHM /PL
68 PWR_SW#
V1.2
PR8957 100KOhm /PL
30 EPX_GATE_EC#
69 EPX_GATE_SW#
PD8935 BAT54CW /PL/X
PR8920 0Ohm /X
PR8951 0Ohm /PL
0-Ohm
ADP_IN
A/D_DOCK_IN
PC8951 0.22UF/25V /PL
PR8921 100KOhm /PL
0.22u
PR8988 390KOhm /PL
PQ8977A UM6K1N /PL
PR8956 0Ohm /PL/X
88 AC_APR_UC_10
V1.2 For ADP power latch
BAT_IN
V1.3
BAT
PQ8977B UM6K1N /PL
PR8990 100KOhm
PC8949 0.22UF/25V /X
PR8989X 510KOhm /X
V1.2
PWR_SW#
80ms (min)
+3VA
?
40ms (max)
PS-ON
Title : <Title>
ASUSTeK COMPUTER INC.
Engineer: CH/Fred
Size B
Project Name UL80VT
Rev 3.12
Date: Monday, May 24, 2010
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PEGATRON Title : POWER_PROTECT

MJ2-Power Div-Power Dept.2 Engineer: Jam_Chang

Size	Project Name	Rev
D	ULSOVT	3.1C

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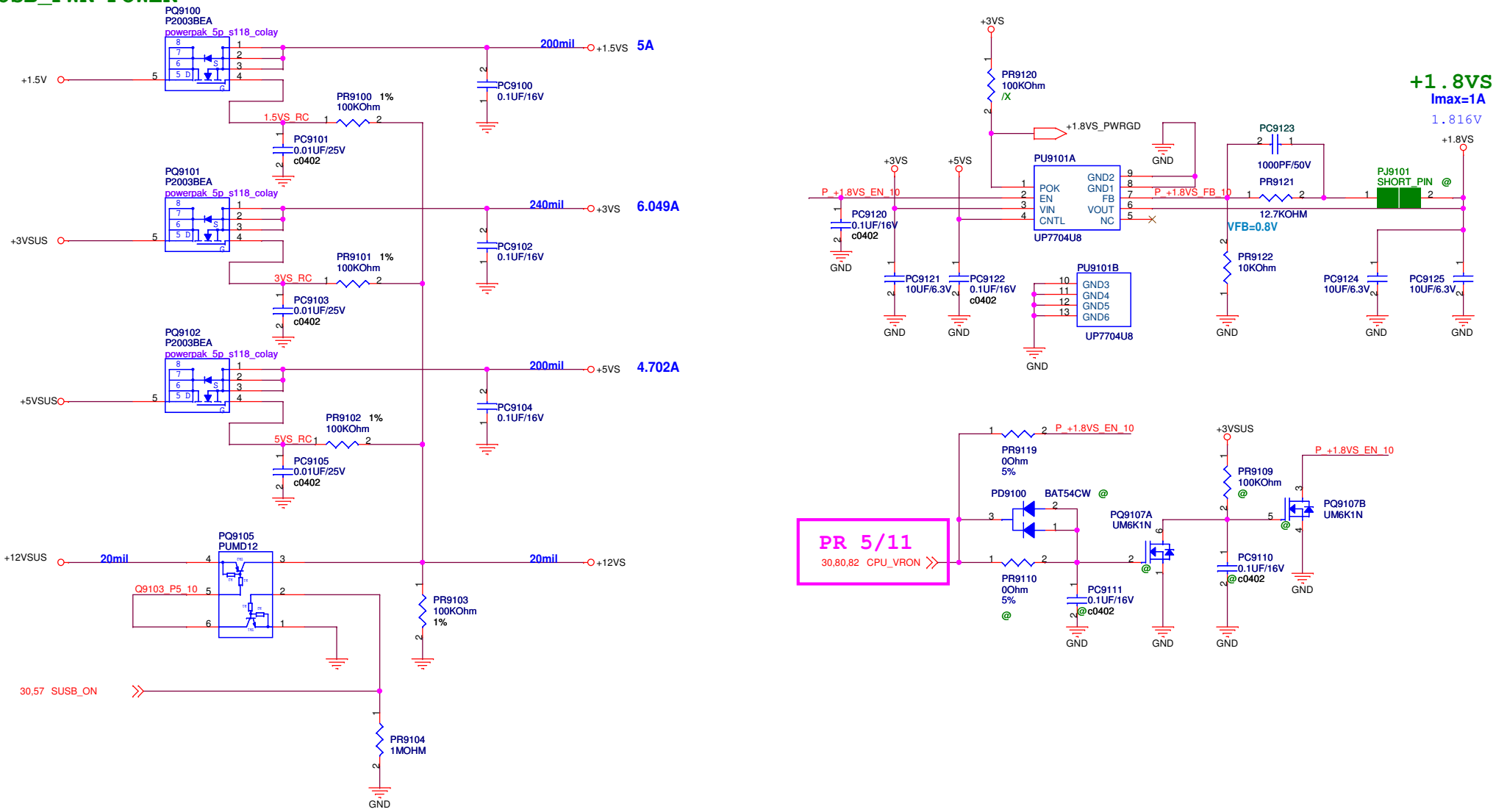
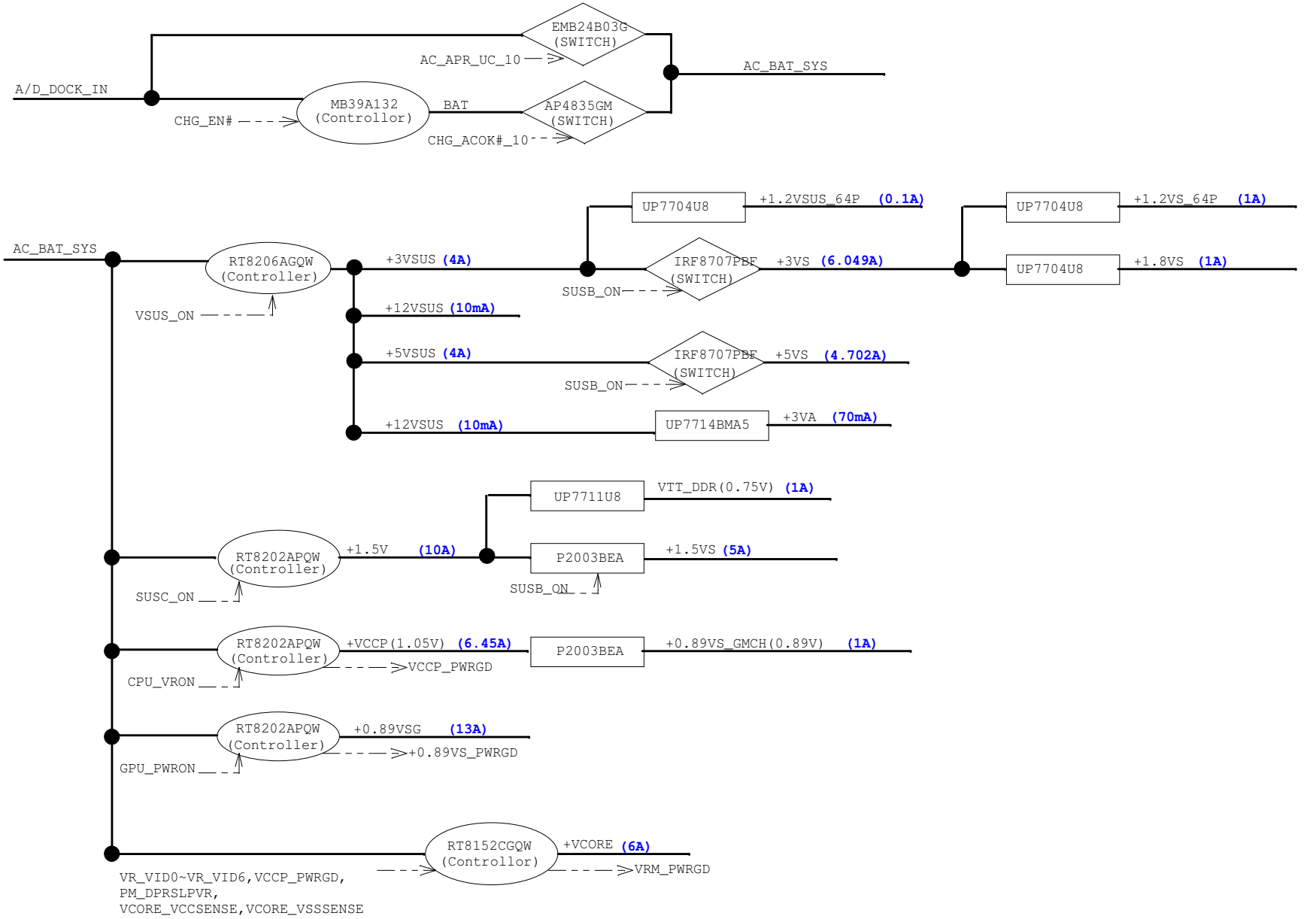
SUSB_PWR POWER



<Variant Name>

ASUSTeK COMPUTER INC. NB	Title: POWER_LOAD SWITCH	
	Engineer: Matt_Wang	
Size: B	Project Name: Design_IP	Rev: 1.0
Date: Monday, May 24, 2010	Sheet 91 of 97	



<Variant Name>

Title : POWER FLOW

ASUSTek Computer Inc.

Engineer: Joy_ZHOU

Size	Project Name	Rev
C	1005HT	1.2G

Date: Monday, May 24, 2010 Sheet 92 of 97

PEGATRON	Title : POWER_HISTORY	
BU2-Power Div-Power Dept.2	Engineer: *Ian_Chung*	
Size: C	Project Name: UL80VT	Rev: 3.12
Date: Monday, May 24, 2010	Sheet 93 of 97	

<Variant Name>

Title :0.89VS&+3VS&+5VS

ASUSTek Computer INC.

Engineer: River_Hsu

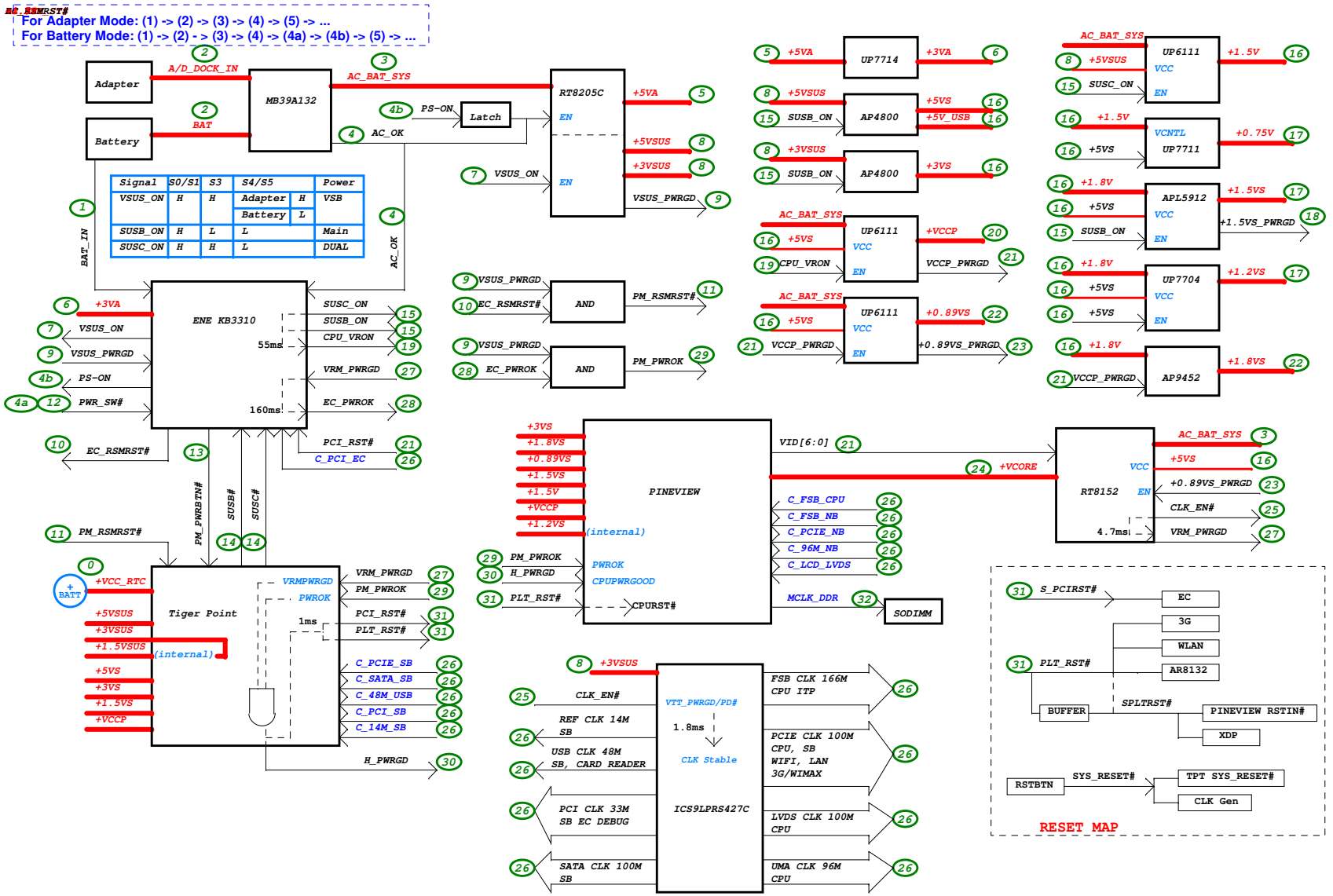
Size	Project Name	Rev
Custom	1005HT	1.2G

Date: Monday, May 24, 2010 | Sheet 94 of 97

ASUSTeK COMPUTER INC. NB3	Title : POWER_PROTECT	
	Engineer: CH_Lin	
Size: C	Project Name: UL30AD	Rev: 1.00
Date: Monday, May 24, 2010	Sheet 95 of 97	

3/29 Update to DDR3_Shangyu
3/29 Add J5501 POWER Button/LED Conn._Shangyu
3/29 Add J6901 Express Gate Button Conn._Shangyu
3/30 Add J5602 T/P Conn._Shangyu
3/30 Switch Express Gate & Wifi Button._Shangyu
3/31 Change CPU DDR3 Voltage_Shangyu
3/31 Change Discharge DDR3 Voltage_Shangyu
3/31 Add TP 0Ohm_Shangyu
4/6 Add DC Jack
5/11 P.04 DDR3_PWROK chang to DDR_PWRGD_Kaiyu
5/11 P.91 P_+1.8VS_EN_10 control change to CPU_VRON_Kaiyu
5/12 P.46 add +3VS_LCD dischage_Kaiyu
5/12 P.67 BToB Pin 15,16 change to Pin 42,43_Kaiyu
5/12 P.68 BToB Pin 15,16 change to Pin 42,43_Kaiyu
5/12 P.46 C4626 change to 0.1uF_Kaiyu
5/12 P.60 EMI ESD check Pass D6005 change optional to @_Kaiyu
5/12 P.37 EMI ESD +/-2K Pass D3702/D3703 change optional to @_Kaiyu
5/12 P.81 EMI ESD +/-2K Pass D3702/D3703 change optional to @_Kaiyu
5/13 P.29 C_LAN_25M_R add 8.2K ohm pull Hi_Kaiyu
5/14 P.47 D4702 change optional to @_Kaiyu
5/17 P.29 C_LAN_25M add 33p for EMI_Kaiyu
5/17 P.29 R2932change to 47ohm for EMI_Kaiyu
5/17 P.22 RN2209 change to 47ohm*4 for EMI_Kaiyu
5/17 P.22 C2201 22pF change to 10pF for EMI_Kaiyu
5/17 P.38 MIC_CLK_R add 33P to GND for EMI_Kaiyu
5/17 P.38 MIC_DATA_R add 33P to GND for EMI_Kaiyu
5/17 P.69 J6901 pin3 change conn. to GND_Kaiyu
5/17 Power Modify BOM
 P81 : PR8106 change to 374K 0402 1%
       PR8113 change to 374K 0402 1%
 P83 : Del PR8305 PJP8300 PC8316
       PR8301 change to 22K 0402 1%
       PR8302 change to 20K 0402 1%
       PR8311 change to 300K 0402 1%
       PR8316 change to @
 P85 : PR8501 change to 12K 0402 1%
       PR8506 change to 100-OHM 0402 1%
5/17 P.61 all part optional change to @_Kaiyu
5/18 P.67 BToB Pin 15,16 & 42,43 Swap(change back)_Kaiyu
5/18 P.68 BToB Pin 15,16 & 42,43 Swap(change back)_Kaiyu
5/18 P.52 add R5254 pullhi to +3Vsus for BIOS detect_Kaiyu
5/18 P.50 SWAP RN5001A & add RN5001B for Layout Request_Kaiyu
IO 5/19 P.40 U6903,U6903 Change to 06G030099010 for NB design ip_Kaiyu
IO 5/19 P.33 L3302 Change to 09G028473401 for cost down_Kaiyu
IO 5/19 P.33 U3_PPON1,U3_PPON2 pull 100K to VSUS_3V3_Kaiyu
5/19 P.70 L7001 change PN to 09G013120103_Kaiyu
5/19 P.91 PC9120 optional change to @_Kaiyu

ASUSTeK COMPUTER INC.	Title : HISTORY	
	Engineer: Max lin	
Size: Custom	Project Name: UL80VT	Rev: 3.12
Date: Monday, May 24, 2010	Sheet 96 of 97	



<Variant Name>

Title : Power Sequence

ASUSTek Computer INC.

Engineer: C. A. Lai

Size	Project Name	Rev
C	1005P	1.2G

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